Errata

Title & Document Type: 8753E RF Vector Network Analyzer Service Manual

Manual Part Number: 08753-90000

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

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Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

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Service Equipment and Analyzer Options

Table of Service Test Equipment

Table 1-1. Required Tools

T-8, T-10, T-15, T-20, and T-25 TORX screwdrivers
Flat-blade screwdrivers-small, medium, and large
5/16-inch open-end wrench (for SMA nuts)
2-mm extended bit allen wrench
3/16, 5/16, and 9/16-inch hex nut drivers
5/16-inch open-end torque wrench (set to 10 in-lb)
2.5-mm hex-key driver
Non-conductive and non-ferrous adjustment tool
Needle-nose pliers
Tweezers
Antistatic work mat with wrist-strap

Table 1-2. Service Test Equipment

Required Equipment	Critical Specifications	Recommended Model	Use*
Spectrum Analyzer	Freq. Accuracy ±7 Hz	HP 8563E	A, T
Frequency counter	Frequency: 300 kHz - 3 GHz (6 GHz for Option 006)	HP 5350B	P
Synthesized Sweeper	Maximum spurious input: < -30 dBc Residual FM: < 20 kHz	HP 83620A	P
Oscilloscope	Bandwidth: 100 MHz Accuracy: 10%	any	T
Digital Voltmeter	Resolution: 10 mV	any	T
Tool Kit	No substitute	HP part number 08753-60023	T
Power Meter (HP-IB)		HP 436A/437/438A	A, P, T
Power Meter (HP-IB)	Single channel, 437B emulation mode	EPM-441A	A, P, T
Power Sensor	Frequency: 300 kHz-3 GHz, 50 ohm	HP 8482A	A, P, T
Power Sensor (for Option 006)	Frequency: 3 GHz-6 Ghz	HP 8481A	A, P, T
Power Sensor	Frequency: 300 kHz-3 GHz, 75 ohm	HP 8483A Opt. H03	A, P
Photometer		Tektronix J16	A
Photometer Probe		Tektronix J6503	A
Light Occluder		Tektronix 016-0305-00	A
Printer		HP ThinkJet, DeskJet, LaserJet	P
Floppy Disk	3.5-inch	HP 92192A (box of 10)	A
Calibration Kit 7 mm, 50 ohm	No substitute	HP 85031B	P
Calibration Kit Type-N, 75 ohm	No substitute	HP 85036B	P
Verification Kit 7 mm	No substitute	HP 85029B	P
Low Pass Filter	>50 dB @ 2.96 Hz and passband that includes 800 Mhz	HP P/N 9135-0198	A
Step Attenuator	No substitute	HP 8498A Opt. 001, H18	P

* P - Performance Tests
A - Adjustment
T - Troubleshooting

Table 1-2. Service Test Equipment (2 of 3)

Required Equipment	Critical Specifications	Recommended Model	Use*
Attenuators (fixed):	Return loss: ≥dB APC-7 20 dB (2)	HP 8492A Opt. 020	P, T
Attenuators (fixed):	Type-N 20 dB (2)	HP 8491A Opt. 020	P, T
Power Splitter	2-Way, 50Ω	HP 11667A	P, T
Minimum Loss Pad	Type-N, 50 ohm to 75 ohm	HP 11852B	P, T, A
Adapter	APC-7 to Type-N (f)	HP 11524A	A, P
Adapter	APC-7 to Type-N (m)	HP 11525A	A, P
Adapter	APC-7 to 3.5 mm (m)	HP P/N 1250-1746	A, P
Adapter	APC-7 to 3.5 mm (f)	HP P/N 1250-1747	A, P
Adapter	BNC to Alligator Clip	HP P/N 8120-1292	A
Adapter	APC-3.5 (m) to Type-N (f)	HP P/N 1250-1750	A, P
Adapter	APC-3.5 (f) to Type-N (f)	HP P/N 1250-1745	A, P
Adapter	BNC (m) to Type-N (f)	HP P/N 1250-1477	P
Adapter	Type-N (f) to Type-N (f)	1250-0777	P
RF Cable (2 each)	24-inch, APC-7	HP P/N 8120-4779	A, P
RF Cable Set	APC-7, 50Ω	HP 11857D	A, P
RF Cable	24-inch, APC-7, 50 ohm (2)	HP P/N 8120-4779	P, A
RF Cable	24-inch, Type-N, 75 ohm (2)	HP P/N 8120-2408	A, P
RF Cable	24-inch Type-N, 50 ohm (2)	HP P/N 8120-4781	A, P
RF Cable Set	Type-N, 50Ω	HP 11851B	P, A
HP-IB Cable		HP 10833A/B/C/D	A
Coax Cable	BNC	HP P/N 8120-1840	A
Coax Cable	BNC (m) to BNC (m), 50Ω	HP 10503A	A

* P - Performance Tests
A - Adjustment
T - Troubleshooting

Table 1-2. Service Test Equipment (3 of 3)

Required Equipment	Critical Specifications	Recommended Model	Use*
Antistatic Wrist Strap		HP P/N 9300-1367	A, T, P
Antistatic Wrist Strap Cord		HP P/N 9300-0980	A, T, P
Static-control Table Mat and Earth Ground Wire		HP P/N 9300-0797	A, T, P
Non-Metalic Adjustment Tool		HP P/N 8830-0024	A
BNC Alligator Clip Adapter		HP P/N 8120-1292	A
BNC-to-BNC Cable		HP P/N 8120-1840	A

* P - Performance Tests
A - Adjustment
T - Troubleshooting

Principles of Microwave Connector Care

Proper connector care and connection techniques are critical for accurate, repeatable measurements.

Refer to the calibration kit documentation for connector care information. Prior to making connections to the network analyzer, carefully review the information about inspecting, cleaning, and gaging connectors.

Having good connector care and connection techniques extends the life of these devices. In addition, you obtain the most accurate measurements.

This type of information is typically located in Chapter 3 of the calibration kit manuals.

For additional connector care instruction, contact your local Hewlett-Packard Sales and Service Office about course numbers HP 85050A+24A and HP 85050A + 24D.

See the following table for quick reference tips about connector care.

Table 1-3. Connector Care Quick Reference

Handling andStorage	
Do	**Do Not**
Keep connectors clean	**Touch mating-planesurfaces**
Extend sleeve or connector nut	**Set connectors contact-end down**
Use plastic end-caps during storage	
Visual Inspection	
Do	**Do Not**
Inspect all connectors carefully	Use a damaged connector—ever
Look for metal particles, scratches, and dents	
Connector Cleaning	
Do	**Do Not**
Try compressed air first	Use any abrasives
Use isopropyl alcohol	Get liquid into plastic support beads
Clean connector threads	
Gaging Connectors	
Do	**Do Not**
Clean and zero the gage before use	Use an out-of-spec connector
Use the correct gage type	
Use correct end of calibration block	
Gage all connectors before first use	
Making Connections	
Do	**Do Not**
Align connectors carefully	Apply bending force to connection
Make preliminary connection lightly	**Over tighten preliminary connection**
Turn only the connector nut	**Twist or screw any connection**
Use a torque wrench for final connect	**Tighten past torque wrench "break" point**

Analyzer Options Available

Option 1D5, High Stability Frequency Reference

This option offers ±0.05 ppm temperature stability from 0 to 60° C (referenced to 25° C).

Option 002, Harmonic Mode

This option provides measurement of second or third harmonics of the test device' s fundamental output signal. Frequency and power sweep are supported in this mode. Harmonic frequencies can be measured up to the maximum frequency of the receiver. However, the fundamental frequency may not be lower than 16 MHz.

Option 006, 6 GHz Operation

This option extends the maximum source and receiver frequency of the analyzer to 6 GHz.

Option 010, Time Domain

This option displays the time domain response of a network by computing the inverse Fourier transform of the frequency domain response. It shows the response of a test device as a function of time or distance. Displaying the reflection coefficient of a network versus time determines the magnitude and location of each discontinuity. Displaying the transmission coefficient of a network versus time determines the characteristics of individual transmission paths. Time domain operation retains all accuracy inherent with the correction that is active in of such devices as SAW filters, SAW delay lines, RF cables, and RF antennas.

Option 011, Receiver Configuration

This option allows front panel access to the R, A, and B samplers and receivers. The transfer switch, couplers, and bias tees have been removed. Therefore, external accessories are required to make most measurements.

Option 075, 75 ohm Impedance

This option offers 75 ohm impedance bridges with type-N test port connectors.

Option 1DT, Delete Display

This option removes the built-in flat panel display, allowing measurement results to be viewed with an external VGA monitor only.

Option 1CM, Rack Mount Flange Kit Without Handles

This option is a rack mount kit containing a pair of flanges and the necessary hardware to mount the instrument, with handles detached, in an equipment rack with 482.6 mm (19 inches) horizontal spacing.

Option 1CP, Rack Mount Flange Kit With Handles

This option is a rack mount kit containing a pair of flanges and the necessary hardware to mount the instrument with handles attached in an equipment rack with 482.6 mm (19 inches) spacing.

Service and Support Options

The analyzer automatically includes a three-year warranty for repair at a Hewlett-Packard facility.

The following service and support options are also available. Contact your local sales or service office.

Option W32

This option provides three years of return to HP calibration service.

Option W34

This option provides three years of return to HP Standards Compliant Calibration.

2

System Verification and Performance Tests

There are two ways to confirm that the HP 8753E network analyzer is able to make measurements as specified by Hewlett-Packard. Both ways are described in this chapter.

The first way is through the system verification procedure. With system verification, the performance of the network analyzer is confirmed as a complete measurement system. The network analyzer is used to measure the traceable behavior of test devices that are part of a verification kit. All the measurement uncertainties of the network analyzer, taken as a measurement system, have been accounted for in the serialized data disk shipped with the verification kit.

The specified performance of the network analyzer can also be confirmed using the series of performance tests described in this chapter. Successful completion of an individual test confirms the specified performance of the specific subsystem tested, such as the source or receiver. Successful completion of the whole series of performance tests confirms the specified performance of the network analyzer as a complete measurement system.

How to Test the Performance of Your Analyzer

To obtain the same quality of performance testing that Hewlett-Packard has administered at the factory, you must perform:

- the system verification procedure

OR

- **all** of the performance test procedures.

This quality of performance testing guarantees that the analyzer is performing within all of the published specifications. Hewlett-Packard will issue a Certificate of Calibration for your analyzer if two conditions are met:

1. Your analyzer passes all the performed tests.
2. The equipment and standards that you used to perform the tests are traceable to a national standards institute.

Note If you have a particular type of measurement application that does not use all of the analyzer's measurement capabilities, you may ask your local Hewlett-Packard Customer Service Center for a subset of specifications that you want verified. However, this does create a potential for making incorrect measurements, by using a different application than what. was specified.

Sections in this Chapter

- **System Verification**
- **Performance Tests**

1. Test Port Output Frequency Range and Accuracy
2. External Source Mode Frequency Range
3. Test Port Output Power Accuracy
4. Test Port Output Power Range and Linearity
5. Minimum R Channel Level
6. Test Port Input Noise Floor Level
7. Test Port Input Frequency Response
8. Test Port Crosstalk
9. Calibration Coefficients

10. System Trace Noise (Only for Analyzers *without* Option 006)
11. System Trace Noise (Only for Analyzers *with* Option 006)
12. Test Port Input Impedance
13. Test Port Receiver Magnitude Dynamic Accuracy
14. Test Port Receiver Magnitude Compression
15. Test Port Receiver Phase Compression
16. Test Port Output/Input Harmonics (Option 002 Analyzers *without* Option 006 only)
17. Test Port Output/Input Harmonics (Option 002 Analyzers *with* Option 006 only)

Performance Test Record

Find and use the appropriate "Performance Test Record" in the following subchapters:

- Performance Test Record for 30 kHz to 3 GHz
- Performance Test Record for 30 kHz to 6 GHz

System Verification Cycle and Kit Re-certification

Hewlett-Packard recommends that you verify your network analyzer measurement system every six months Hewlett-Packard also suggests that you get your verification kit re-certified annually. Refer to *HP 85029B 7-mm Verification Kit Operating and Service Manual* for more information.

Note — The system verification procedures can also apply to analyzers with Option 075 (75 ohm analyzers) if minimum loss pads and type-N (m) to APC-7 adapters are **used.**

Check to see how the verification kit floppy disk is labeled:

- If your verification disk is labeled HP 8753D Verification Data Disk, or HP 8753D & HP 8753E Verification Data Disk, you may proceed with the system verification.
- If your verification disk is not labeled as indicated above, you may send your HP 85029B 7-mm verification kit to the nearest service center for recertification, which includes a data disk that you can use with the HP 87533.

HP 8753E System Verification

Equipment Required

Calibration Kit, 7-mm	HP 85031B
Verification Kit, 7-mm	HP 85029B
Test Port Extension Cable Set, 7-mm	HP 11857D
Printer	HP ThinkJet/DeskJet/LaserJet

Additional Equipment Required for Option 075 Analyzers

Minimum Loss Pad (2), 50 Ohm to 75 Ohm	HP11852B
Adapter (2), APC-7 to Type-N (m)	HP 11525A

Analyzer warmup time: **1 hour**

This system verification consists of three separate procedures:

1. Initialization
2. Measurement Calibration
3. Device Verification

Initialization

1. Connect the equipment as shown in Figure 2-l. Let the analyzer warm up for one hour

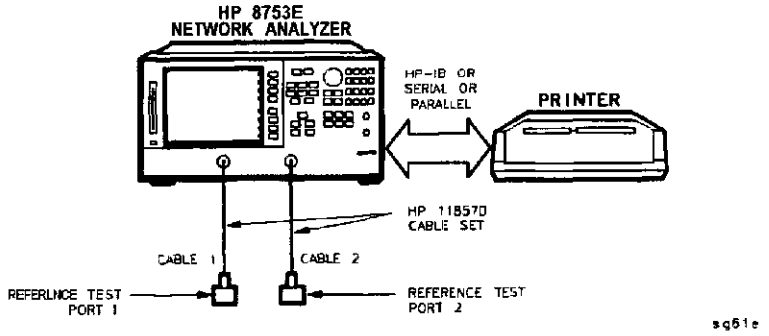


Figure 2-1. System Verification Test Setup

2. While the equipment is warming up, review the "Connector Care Quick Reference" information in Chapter 1. Good connections and clean, undamaged connectors are critical for accurate measurement results.
3. Insert the verification kit disk into the analyzer disk drive.
4. Press (Preset) (Save/Recall) SELECT DISK INTERNAL DISK
5. If you want a printout of the verification data for all the devices, press [SERVICE MENU] TEST OPTIONS] RECORD ON.

Note If you switch on the record function, you CANNOT switch it off during the verification procedure.

6. Position the paper in the printer so that printing starts at the top of the page.
7. If you have difficulty with the printer:
   - If the interface on your printer is HP-IB, verify that the printer address is set to 1 (or change the setting in the analyzer to match the printer).
   - If the interface on your printer is serial or parallel, be sure that you selected the printer port and the printer type correctly (refer to the ***HP 8753E Network Analyzer User's Guide*** for more information on how to perform these tasks).
8. Press (System) SERVICE MENU TESTS SYS VER TESTS [EXECUTE TEST
9. The analyzer displays Sys Ver Init DONE; the initialization procedure is complete.

Caution ***DO NOT*** press [Preset) or recall another instrument state. You must use the instrument state that you loaded during the initialization procedure.

Measurement Calibration

10. Press [CAL] CAL KIT SELECT CAL KIT CAL KIT: 7mm RETURN RETURN CALIBRATE MENU FULL 2-PORT.

11. Press ISOLATION OMIT ISOLATION.

12. Press REFLECTION

13. Connect the "open" end of the open/short combination (supplied in the calibration kit) to reference test port 1, as shown in Figure 2-2.

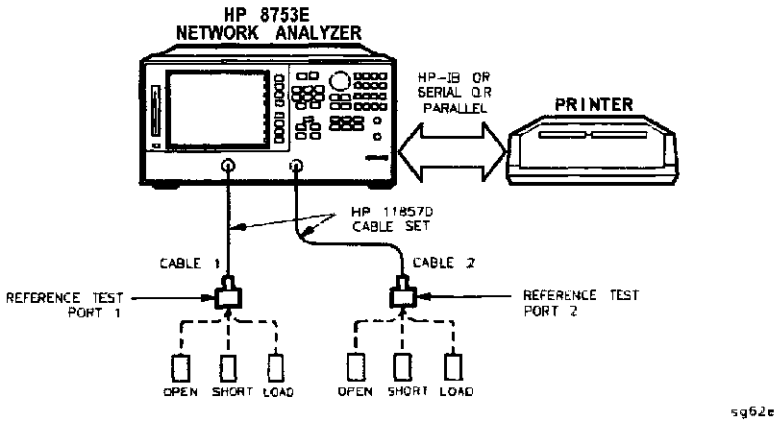


Figure 2-2. Connections for Measurement Calibration Standards

14. Press [FORWARD: OPEN]

15. When the analyzer finishes measuring the standard, connect the "short" end of the open/short combination to reference test port 1.

16. Press FORWARD: SHORT

17. When the analyzer finishes measuring the standard, connect the 50 ohm termination (supplied in the calibration kit) to reference test port 1.

18. Press FORWARD LOAD

19. When the analyzer finishes measuring the standard, connect the "open" end of the open/short combination to reference test port 2.

20. Press REVERSE: OPEN

21. When the analyzer finishes measuring the standard, connect the "short" end of the open/short combination to reference test port 2.

22. Press REVERSE SHORT.

23. When the analyzer finishes measuring the standard, connect the 50 ohm termination to reference test port 2.

24. Press REVERSE LOAD

25. When the analyzer finishes measuring the standard, press STANDARDS DONE

The analyzer briefly displays COMPUTING CAL COEFFICIENTS.

26. Connect the test port cables as shown Figure 2-3.

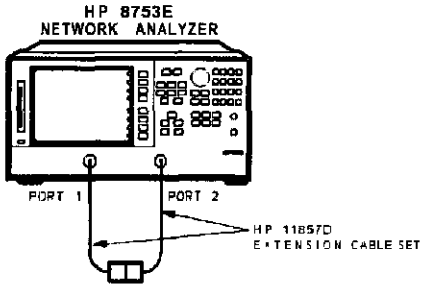


Figure 2-3. Transmission Calibration Setup

27. Press TRANSMISSION DO BOTH FWD + REV.

28. Press [DONE 2-PORT CAL.

29. Press (Save/Recall) SELECT DISK INTERNAL MEMORY RETURN SAVE STATE to save the calibration into the analyzer internal memory.

30. When the analyzer finishes saving the instrument state, press SELECT DISK INTERNAL **DISK**.

Device Verification

31 Press [SYSTEM] [SERVICE MENU] TESTS [28] [x1] EXECUTE TEST

32. At the prompt, connect the 20 dB attenuator (supplied in the verification kit) as shown in Figure 2-4.

33. Press CONTINUE to run the test:

- If you switched OFF the record function, you have to press [CONTINUE] after each S-parameter measurement.
- If you switched ON the record function, the analyzer measures all S-parameters (magnitude and phase) without pausing. Also, the analyzer only displays and prints the PASS/FAIL information for the S-parameter measurements that are valid for system verification.

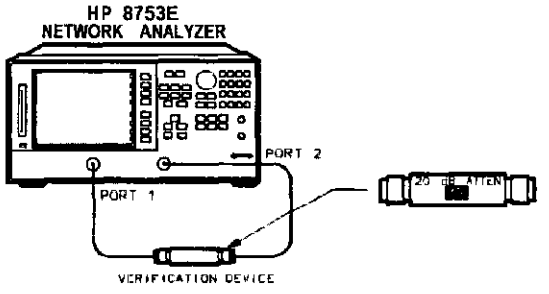


Figure 2-4. Connections for the 20 dB Verification Device

34. When the analyzer finishes all the measurements, connect the 50 dB attenuator (supplied in the verification kit), as shown in Figure 2-5.

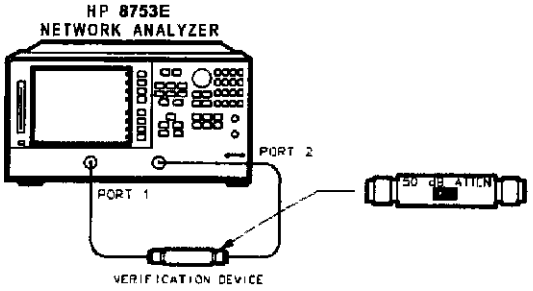


Figure 2-5. Connections for the 50 dB Verification Device

35. Press (shift) (29) [x1] EXECUTE TEST [CONTINUE] .

36. When all measurements are complete, replace the verification device with the verification mismatch, as shown in Figure 2-6. Be sure that you connect Port A of the verification mismatch to reference test port 1.

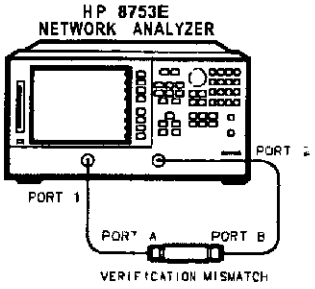
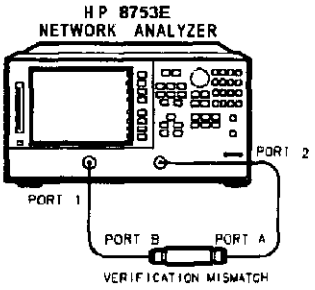


Figure 2-6. Mismatch Device Verification Setup 1

37. Press RETURN TESTS [30] [x1] EXECUTE TEST **[CONTINUE]** .

38. When the analyzer finishes all the measurements, connect the mismatch verification device, as shown in Figure 2-7. Notice that Port B is now connected to reference test port 1.



sg67e

Figure 2-7. Mismatch Device Verification Setup 2

39. Press RETURN TESTS [31] (xl) [EXECUTE TEST [CONTINUE] .

40. You have completed the system verification procedure when the analyzer displays Ver Def 4 DONE.

In Case of Difficulty

1. Inspect all connections.

Caution DO NOT disconnect the cables from the analyzer test ports. Doing so WILL ***INVALIDATE*** the calibration that you have done earlier.

2. Press [PRESET] [SAVE/RECALL] [SELECT DISK] [INTERNAL MEMORY] [RETURN] . Using the front panel knob, highlight the title of the full 2-Port calibration that you have done earlier, then press RECALL STATE
3. Repeat the "Device Verification" procedure.
4. If the analyzer still fails the test, check the measurement calibration as follows·
   a. Press [PRESET].
   b. Recall the calibration by pressing [SAVE/RECALL] SELECT DISK [INTERNAL MEMORY] [RETURN].
   c. Use the front panel knob to highlight the calibration you want to recall and press RECALL STATE
   d. Connect the short to reference test port 1.
   e. Press [MEAS] [Refl: FWD Sll (A/R)] [MENU] TRIGGER MENU] [CONTINUOUS] .
   f. Press [SCALE REF] [SCALE/DIV] [.05] [x1].
   g. Check that the trace response is 0.00 ± 0.05 dB.
   h. Disconnect the short and connect it to reference test port 2.
   i. Press [MEAS] [Refl: REV S22 (B/R)]
   j. Check that the trace response is 0.00 ±0.05 dB.
   k. If any of the trace responses are out of the specified limits, repeat the "Measurement Calibration" and "Device Verification" procedures.
5. Refer to Chapter 4, "Start Troubleshooting Here," for more troubleshooting information.

1. Test Port Output Frequency Range and Accuracy

Specifications

Frequency Range	Frequency Accuracy[1]
30 kHz to 3 GHz	±10 ppm
3 GHz to 6 GHz[2]	±10 ppm

1 At 25° C ±5° C.

2 Only for analyzers with Option 006 - 30 kHz to 6 GHz range

Required Equipment

Frequency Counter (30 kHz to 500 MHz)	HP 5350B/51B/52B
Frequency Counter (500 MHz to 6 GHz)	.HP 5350B/51B/52B
Cable, 50 Ohm Type-N, 24-inch	.HP P/N 8120-4781
Adapter, APC-3.5 (f) to Type-N (f)	HP P/N 1250-1745
Adapter, APC-7 to Type-N (f)	HP P/N 11524A
Adapter, Type-N (f) to BNC (m)	HP P/N 1250-1477

Additional equipment needed for an 87533 with Option 075

Minimum Loss Pad, 50 Ohm to 75 Ohm	HP 11852B

Analyzer warmup time: 30 minutes

Perform this test to verify the frequency accuracy of the HP 87533 over its entire operating frequency range.

1. Connect the equipment as shown in Figure 2-8.

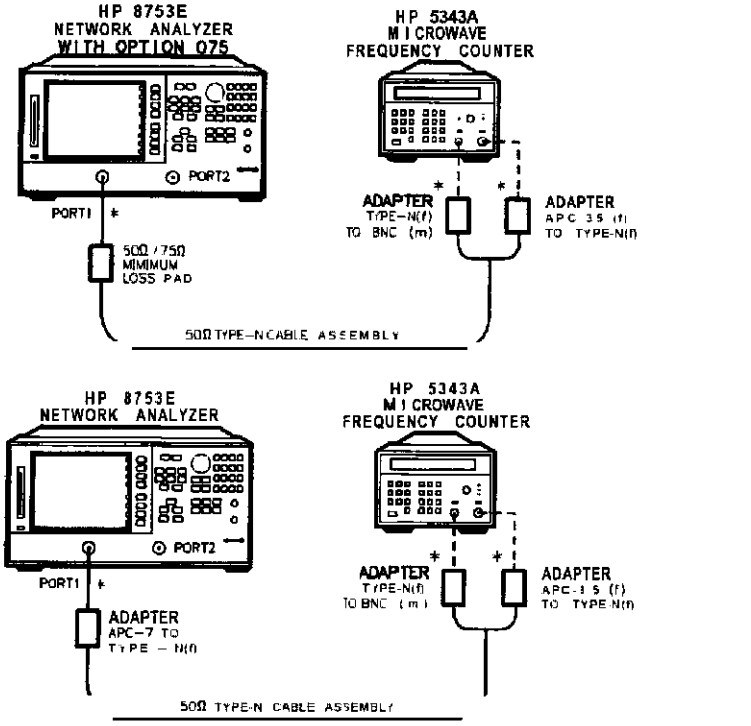


Figure 2-8. Test Port Output Frequency Range and Accuracy Test Setup

2. Press (Preset) (Menu) **CW FREQ**.
3. Press (30) (k/m) and write the frequency counter reading on the "Performance Test Record."
4. Repeat step 3 for each instrument frequency listed in the "Performance Test Record."

In Case of Difficulty

1. If any measured frequency is close to the specification limits, check the time base accuracy of the counter used.
2. If the analyzer fails by a significant margin at all frequencies (especially if the deviation increases with frequency), the master time base probably needs adjustment. In this case, refer to the "Frequency Accuracy Adjustment" procedure, located in Chapter 3, "Adjustments and Correction Constants." The "Fractional-N Frequency Range Adjustment" also affects frequency accuracy.
3. Refer to Chapter 7, "Source Troubleshooting," for related troubleshooting information.

2. External Source Mode Frequency Range

Specifications

Frequency Range
30 kHz to 3 GHz
30 kHz to 6 GHz[1]

1 Only for analyzers with Option 006 – 30 kHz to 6 GHz range.

Equipment Required

External Source ..... HP 83620 A
Cable, APC-7, 24-inch ..... HP P/N 8120-4779
Adapter, APC-3.5 (f) to APC-7 ..... HP P/N 1250-1747
Adapter, APC-3.5 (m) to APC-7 ..... HP P/N 1250-1746

Analyzer warmup time: 30 **minutes**

Perform this test to verify that the analyzer's reference channel, input R, is capable of phase locking to an external CW signal.

1 On the external source, press (Preset) [redacted] [POWER LEVEL] [−/−] [20][GHz/dB(m)].

2. Connect the equipment as shown in Figure 2-9.

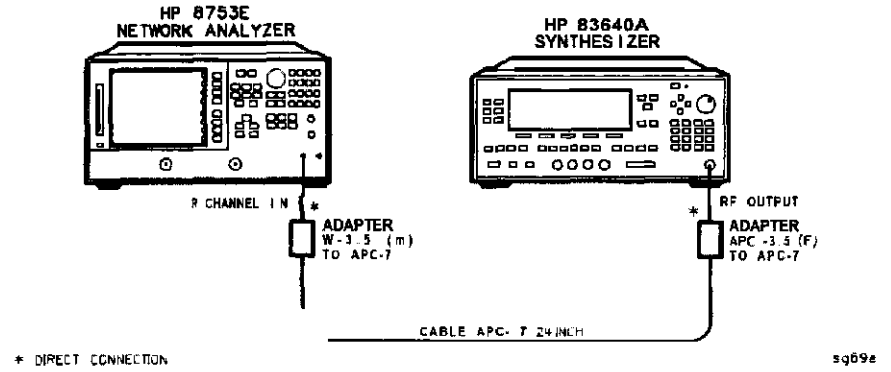


Figure 2-9. External Source Mode Frequency Range Test Setup

3. On the network analyzer, press [PRESET] [MEAS] INPUT PORTS R

4. Press (System) INSTRUMENT MODE EXT SOURCE AUTO (Menu) CW FREQ (10) (M/μ).

5. Check to see if the analyzer is phase locking to the external CW signal:
   - If the analyzer displays any phase lock error messages, write "unlock" in the "Performance Test Record" for the set CW signal.
   - If the analyzer does not display any phase lock error messages, write "lock" in the "Performance Test Record" for the set CW signal.

6. On the external source, press [RQS/SRQ] [MHz]

7. On the analyzer, press [20] [MHz]

8. Repeat step 5 through 7 for the other external source CW frequencies listed in the "Performance Test Record."

In Case of Difficulty

If the analyzer displayed any phase lock error messages:

1. Be sure the external source power is set within 0 to -25 dBm.
2. Make sure the analyzer's "Ext **Source** Auto" feature is selected. In addition, verify that the analyzer is set to measure its input channel R.
3. Verify that all connections are tight.

3. Test Port Output Power Accuracy

Specifications

Frequency Range	Test Port Output Power Accuracy[1]
300 kHz to 3 GHz	±1.0 dB
3 GHz to 6 GHz[2]	±1.0 dB

1 At 0 dBm and 25° C ±5° C

2 Only for analyzers with Option 006 - 30 kHz to 6 GHz range

Equipment Required for 50 Ohm Analyzers

Power Meter HP 436A/437B/438A
Power Sensor HP8482A
Adapter, APC-7 to Type-N (f) HP 11524A

Additional Equipment Required for Analyzers with Option 006

Power Sensor ..... HP 8481A

Equipment Required for 75 Ohm Analyzers

Power Meter HP 436A/437B/438A
Power Sensor HP 8483A Option HO3

Analyzer warmup time: 30 **minutes**

Perform this test to confirm the accuracy of the HP 87533 source output power.

1. Zero and calibrate the power meter. For more information of how to perform this task, refer to the power meter operating manual.
2. Connect the equipment as shown in Figure 2-10.

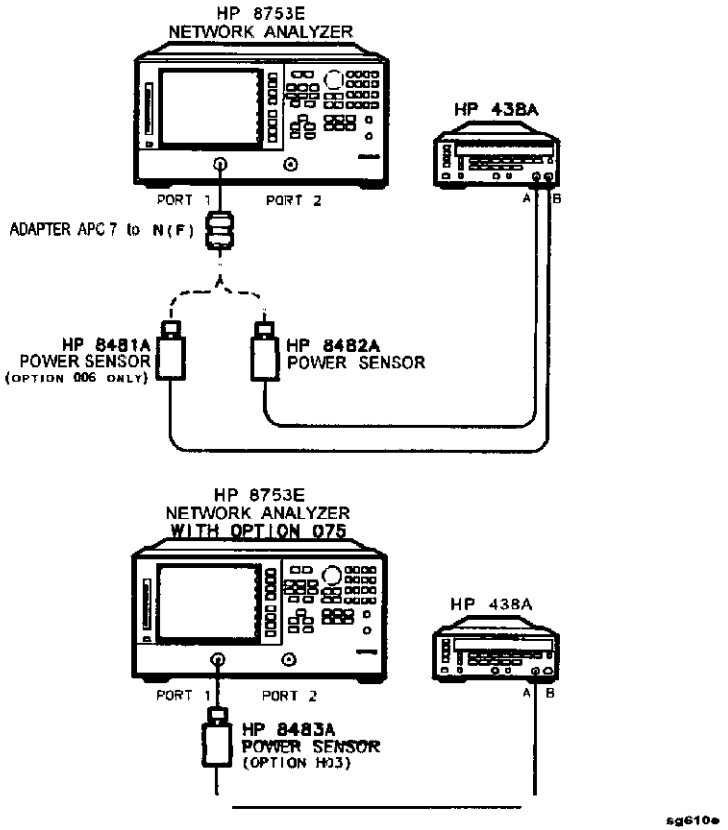


Figure 2-10. Source Output Power Accuracy Test Setup

3. Press [PRESET].

Note The factory preset test port power is 0 dBm.

4. Press [MENU] CW FREQ [300] [k/m]. Set the calibration factor on the power meter for this CW frequency.
5. Write the power meter reading on the "Performance Test Record."
6. Repeat steps 4 and 5 for each CW frequency listed in the "Performance Test Record." For analyzers with Option 006, use the HP 8481A power sensor for all frequencies above 3 GHz.

In Case of Difficulty

1. Be sure the source power is switched on. Press [MENU] POWER. Check the SOURCE PWR softkey; "on" ***should*** be highlighted. Otherwise, press [SOURCE PWR] to switch on the source power.
2. Refer to Chapter 7, "Source Troubleshooting," for more troubleshooting information.

4. Test Port Output Power Range and Linearity

Specifications

Power Range	Power Level Linearity[1]
−15 to +5 dBm	±0.2 dB
+5 to +10 dBm	±0.5 dB

1 Relative to 0 dBm output level.

Required Equipment

Power Meter ..... HP 437B/438A
Power Sensor ..... HP 8482A
Adapter, APC-7 to Type-N (f) ..... HP 11524A

Additional Required Equipment for Analyzers with Option 006

Power Sensor ..... HP 8481A

Additional Required Equipment for Analyzers with Option 075

Power Sensor ..... HP 8483A Option HO3

Analyzer warmup time: **1 hour**

Perform this test to verify the analyzer's test port output power range and power level linearity at selected CW frequencies.

1. Zero and calibrate the power meter. Refer to the power meter operating manual for more information on how to do this task.
2. On the network analyzer, press (Preset) (Menu) CW **FREQ** (300) (k/m). Set the power meter calibration factor for this CW frequency.
3. Connect the equipment as shown in Figure 2-11.

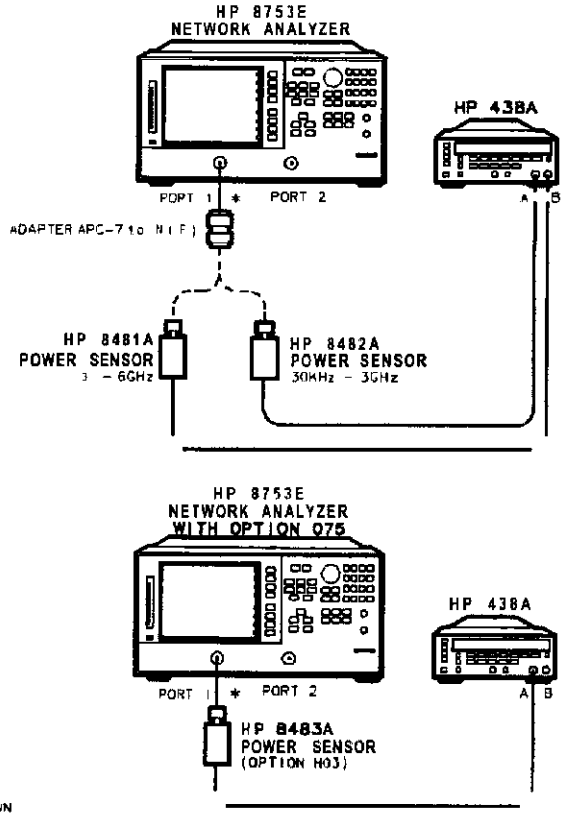


Figure **2-11. Test Port Output Power Range and Accuracy Test Setup**

4. On the HP 438A, press (REL). This sets the current power level for relative power measurement.
5. On the network analyzer, press (Menu] POWER PWR RANGE MAN.
6. Write the power meter reading in the "Results Measured" column on the "Performance lest Record. "
7. Calculate the difference between the analyzer test port power (which appears on the analyzer's display) and the power meter reading. Write the result in the "Power Level Linearity" column on the "Performance Test Record."
8. Repeat steps 5 through 7 for the other power levels listed in the "Performance Test Record. "
9. Press (Menu) CW FREQ (3) (G/n).
10. Set the power meter calibration factor for this CW frequency and press (REL) to set the reference at this new frequency.
11. Press (Menu) POWER (-15) (x1).
12. Write the power meter reading in the "Results Measured" column on the "Performance Test Record. "
13. Calculate the difference between the analyzer test port power and the power meter reading. Write the result in the "Power Level Linearity" column of the "Performance Test Record."
14. Repeat steps 11 through 13 for the other power levels listed in the "Performance Test Record."

In Case of Difficulty

1. Ensure that the power meter and power sensor(s) are operating to specifications. Be sure you set the power meter calibration factor for the CW frequency that you are testing.
2. Verify that there is power coming out of the analyzer's test port 1. Be sure you did not accidentally switch off the analyzer's internal source. If you did so, press (Menu) POWER SOURCE PWR ON.
3. Repeat this performance test.

5. Minimum R Channel Level

Specifications

Frequency Range	Minimum R Channel Level
300 kHz to 3 GHz	<−35 dBm
3 GHz to 6 GHz[1]	<−30 dBm

1 Only for analyzers with Option 006 – 30 kHz to 6 GHz range

Required Equipment for 50Ω Analyzers

Adapter, APC-3.5 (m) to APC-7 ..... HP P/N 1250-1746
Cable, APC-7 24-inch ..... HP P/N 8120-4779

Required Equipment for 75Ω Analyzers (Option 075)

Minimum Loss Pad, 50Ω to 75Ω ..... HP 11852B
Cable, 50Ω Type-N, 24-inch ..... HP P/N 8120-4781
Adapter, APC-3.5 (m) to Type-N (f) ..... HP P/N 1250-1750

Analyzer warmup time: 1 hour

Perform this test to determine the minimum R channel input power level at which phase lock can be accomplished

1. Connect the equipment as shown in Figure 2-12.

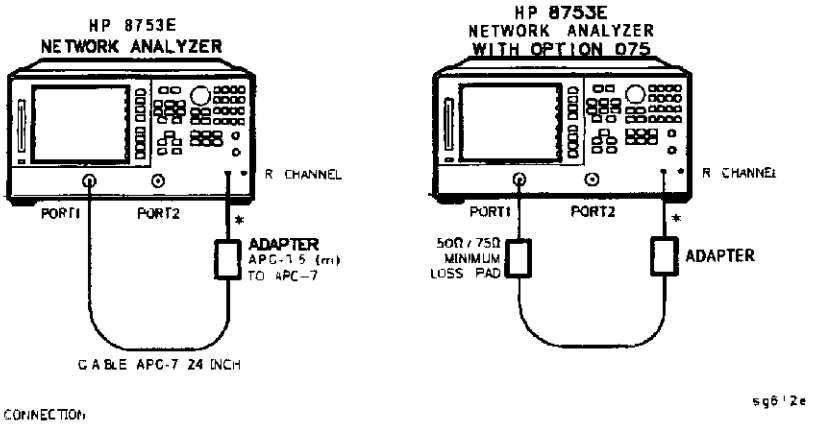


Figure 2-12. Minimum R Channel Level Test Setup

2. Press (Preset) (Meas) INPUT PORTS R

3. Press [Menu) **POWER** PWR RANGE MAN POWER RANGES
   RANGE 4 -55 to -30.

4. Press (Scale Ref) REFERENCE VALUE (-70) (x1).

5. Press (Menu) CW **FREQ** (300) (k/m).

6. Press (Menu) POWER (-65) (x1).
   The analyzer displays the message CAUTION : **NO** IF FOUND : CHECK **R** INPUT LEVEL.

7. Press (↑) to increase the test port power by 1 dBm.

8. If the analyzer displays a phase lock error message, continue increasing the test port power until phase lock is achieved.

9. Write the test port power, that is displayed on the analyzer, on the "Performance Test Record. "

10. Repeat steps 5 through 9 for the other CW frequencies listed in the " Performance Test Record. "

In Case of Difficulty

1. Check the flexible RF cable (W8, as shown in Figure 2-13) between the R sampler assembly (A4) and the All phase lock assembly. Make sure it is connected between A11J1 (PL IF IN) and 1st IF Out.

Caution **Do** *not* push cable W8 down next to the All phase lock assembly.

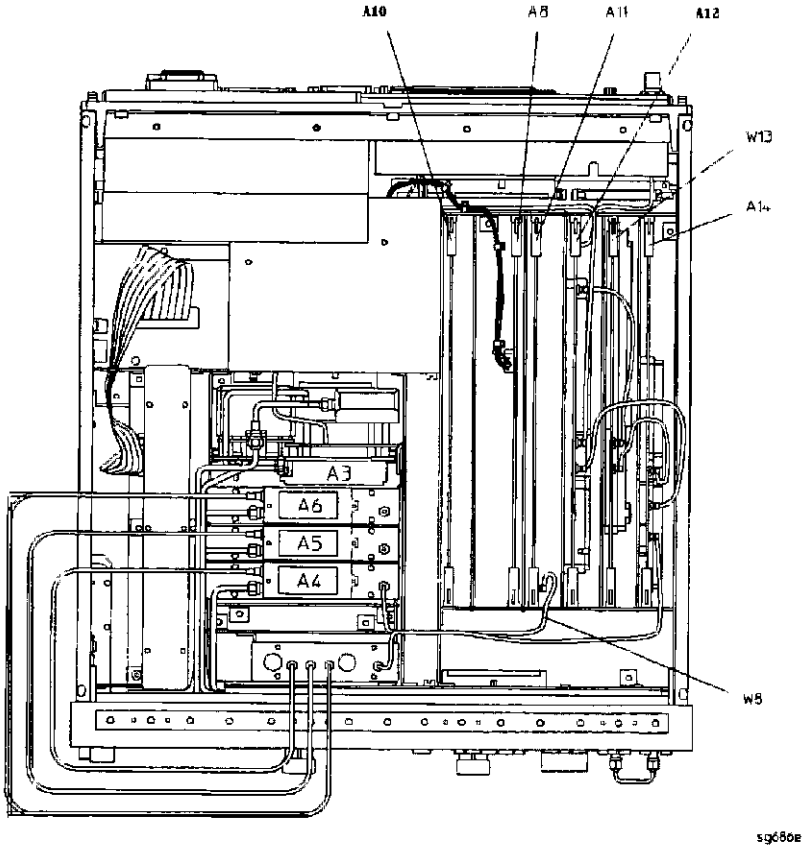


Figure 2-13. Flexible RF Cable Location

2. Using an ohmmeter, verify that the RF cable is not open. In addition, examine both the cable connectors - measure the resistance between the cable center pin and the cable connector and make sure it is ***not*** close to zero.

3. Check the R sampler by substituting it with the B sampler (**A6**).

   a. Move cable W8 to the B sampler (**A6**), as shown in Figure 2-14.

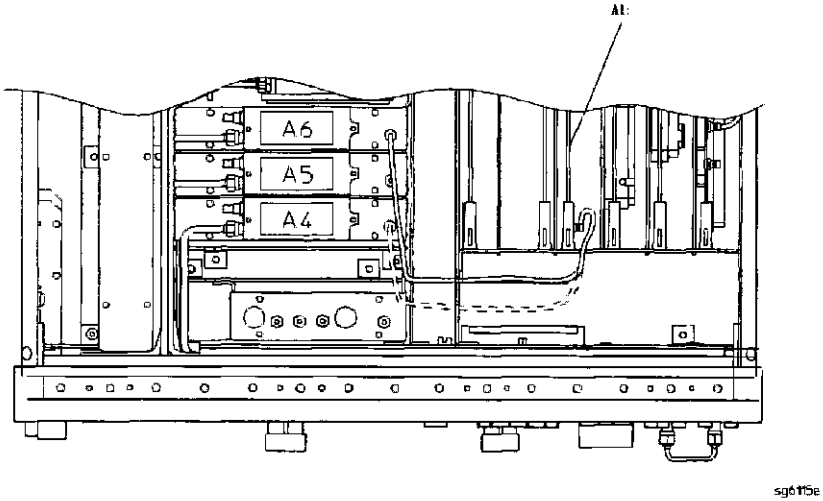


Figure 2-14. Connections for Substituting the R Sampler (A4)

4. Connect the equipment as shown in Figure 2-15.

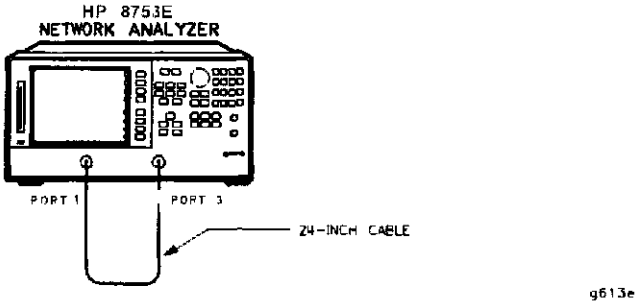


Figure 2-15. Setup for Checking the R Sampler (A4)

5. Repeat the test, but select the B sampler (A6) by pressing (Meas) INPUT PORTS B in step 2. Use the following specifications:

   300 kHz to 3 GHz < −27 dBm
   3 GHz to 6 GHz < −22 dBm

6. If the analyzer fails the test, replace the A11 assembly.
7. Verify that the high/low band adjustments are still within specifications. For more information on how to perform this task, refer to the "High/Low Band Transition Adjustment" located in Chapter 3, "Adjustments and Correction constants."
8. Refer to Chapter 7, "Source Troubleshooting," for more troubleshooting information.

6. Test Port Input Noise Floor Level

Specifications

Frequency Range	Test Port	IF Bandwidth	Average Noise Level
300 kHz to 3.0 GHz	Port 1	3 kHz	−82 dBm
300 kHz to 3.0 GHz	Port 1	10 Hz	−102 dBm
300 kHz to 3.0 GHz	Port 2	3 kHz	−82 dBm
300 kHz to 3.0 GHz	Port 2	10 Hz	−102 dBm
3.0 GHz to 6.0 GHz[1]	Port 1	3 kHz	−77 dBm
3.0 GHz to 6.0 GHz[1]	Port 1	10 Hz	−97 dBm
3.0 GHz to 6.0 GHz[1]	Port 2	3 kHz	−77 dBm
3.0 GHz to 6.0 GHz[1]	Port 2	10 Hz	−97 dBm

1 Only for analyzer with Option 006 - 30 kHz to 6 GHz range.

Equipment Required for 503 Analyzers

Calibration Kit, 7-mm ..... HP 85031B

Equipment Required for 753 Analyzers

Calibration Kit, Type-N ..... HP 85036B

***Analyzer warmup time:* 1 hour**

Perform this test to determine the HP 87533 port 1 and port 2 noise floor levels at the input test ports.

Port 1 Noise Floor Level from 300 kHz to 3 GHz (IF BW = 3 kHz)

1. Connect the equipment as shown in Figure 2-16.

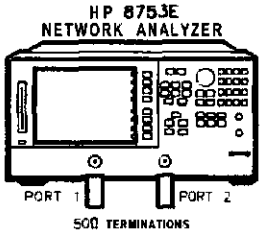


Figure 2-16. Source Input Noise Floor Test Setup

2 Press [Preset] [Avg] IFBW [3000] [x1] [Menu] POWER [-85] [x1] [Stop] [3] [G/n].

3 Press [Meas] INPUT PORTS A TESTPORT 2 [format] LIN MAG [Scale Ref] AUTO SCALE.

4. Press [Marker Fctn] MARKER MODE MENU STATS ON [Menu] TRIGGER MENU SINGLE.

5 When the analyzer finishes the sweep, notice the mean value (which appears on the analyzer display).

6 Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ \text{magnitude mean value})]$$

Note Notice that the mean value that. is displayed on the analyzer is in μUnits. So, for example, if the displayed value is 62 μU, the value that you would put in the equation is (62×10^{-6}).

7. Write this calculated value on the "Performance Test Record."

Port 1 Noise Floor Level from 300 kHz to 3 GHz (IF BW = 10 Hz)

8. Press (Avg) IF BW (10) (x1) to change the IF bandwidth to 10 Hz.

9. Press (Menu) TRIGGER MENU SINGLE

10. When the analyzer finishes the sweep, notice the mean value.

11. Convert the measured linear magnitude mean value to log magnitude, using this equation,

$$Power\ (dBm) = 20 * [\log_{10}(linear\ \text{magnitude}\ mean\ value)]$$

12. Write this calculated value on the "Performance Test Record."

Port 2 Noise Floor Level from 300 kHz to 3 GHz (IF BW = 10 Hz)

13. Press (Meas) INPUT PORTS B TESTPORT 1 (Format) LIN MAG.

14. Press [Menu] TRIGGER MENU SINGLE.

15. When the analyzer finishes the sweep, notice the mean value.

16. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

17. Write this calculated value on the "Performance Test Record."

Port 2 Noise Floor Level from 300 kHz to 3 GHz (IF BW = 3 kHz)

18. Press (Avg) IF BW (3) (k/m) to change the IF bandwidth to 3 kHz.

19. Press (Menu) TRIGGER MENU SINGLE.

20. When the analyzer finishes the sweep, notice the mean value.

21. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

22. Write this calculated value on the "Performance Test Record."

23. This completes the "Test Port Input Noise Floor Level" procedure if your analyzer does not have Option 006. Otherwise continue with the next section.

Port 2 Noise Floor Level from 3 GHz to 6 GHz (IF BW = 3 kHz)

24. Press (Start) (3) (G/n) (Stop) (6) (G/n).

25. Press (Menu) TRIGGER MENU SINGLE.

26. When the analyzer finishes the sweep, notice the mean value.

27. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

28. Write this calculated value on the "Performance Test Record."

Port 2 Noise Floor Level from 3 **GHz** to 6 **GHz** (IF BW = 10 Hz)

29. Press (Avg) IF BW (10) (x1) to change the IF bandwidth to 10 Hz.

30. Press (Menu) **TRIGGER** MENU SINGLE.

31. When the analyzer finishes the sweep, notice the mean value.

32. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

33. Write this calculated value on the "Performance Test Record."

Port 1 Noise Floor Level for 3 **GHz** to 6 **GHz** (IF BW = 10 Hz)

34. Press (Meas) INPUT **PORTS** A **TESTPORT** 2 .

35. Press (Menu) **TRIGGER** MENU SINGLE.

36. When the analyzer finishes the sweep, notice the mean value.

37. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

38. Write this calculated value on the "Performance Test Record."

Port 1 Noise Floor Level from 3 **GHz** to 6 **GHz** (IF **BW** = 3 **kHz**)

39. Press (Avg) IF BW (3) (k/m).

40. Press (Menu) **TRIGGER MENU** SINGLE.

41. When the analyzer finishes the sweep, notice the mean value.

42. Convert the measured linear magnitude mean value to log magnitude, using this equation.

$$Power\ (dBm) = 20 * [\log_{10}(linear\ magnitude\ mean\ value)]$$

43. Write this calculated value on the "Performance Test Record."

In Case of Difficulty

1. Perform the "ADC Linearity Correction Constants (Test 52)," located in Chapter 3, "Adjustments and Correction Constants. "
2. Repeat the "Test Port Input Noise Floor Level" procedure.
3. Suspect the A10 Digital IF assembly if the analyzer fails both test port input noise floor tests.
4. Refer to Chapter 8, "Receiver Troubleshooting," for more troubleshooting information.

7. Test Port Input Frequency Response

Specifications

Frequency Range	Test Port	Input Frequency Response
300 kHz to 3 GHz	Port 1	±1 dB
300 kHz to 3 GHz	Port 2	±1 dB
3 GHz to 6 GHz[1]	Port 1	±2 dB
3 GHz to 6 GHz[1]	Port 2	±2 dB

1 Only for analyzers with Option 006 – 30 kHz to 6 GHz range.

Equipment Required for 50Ω Analyzers

Power Meter . . . . . HP 436A/437B/438A
Power Sensor . . . . . HP 8482A
Cable, APC-7 24-inch . . . . . HP P/N 8120-4779
Adapter, APC-7 to Type-N (f) . . . . . HP 11524A

Additional Equipment Required for Analyzers with Option 006

Power Sensor . . . . . HP 8481A

Equipment Required for 75Ω Analyzers

Power Meter . . . . . HP 436A/437B/438A
Power Sensor . . . . . HP 8483A Option H03
Cable, Type-N . . . . . HP P/N 8120-2408

Analyzer warmup time: **1 hour**

Perform this test to examine the vector sum of all test setup error vectors in both magnitude and phase change as a function of frequency.

Power Meter Calibration for Test Port 1 from 300 kHz to 3 GHz

1. Zero and calibrate the power meter.
2. Connect the equipment as shown in Figure 2-17.

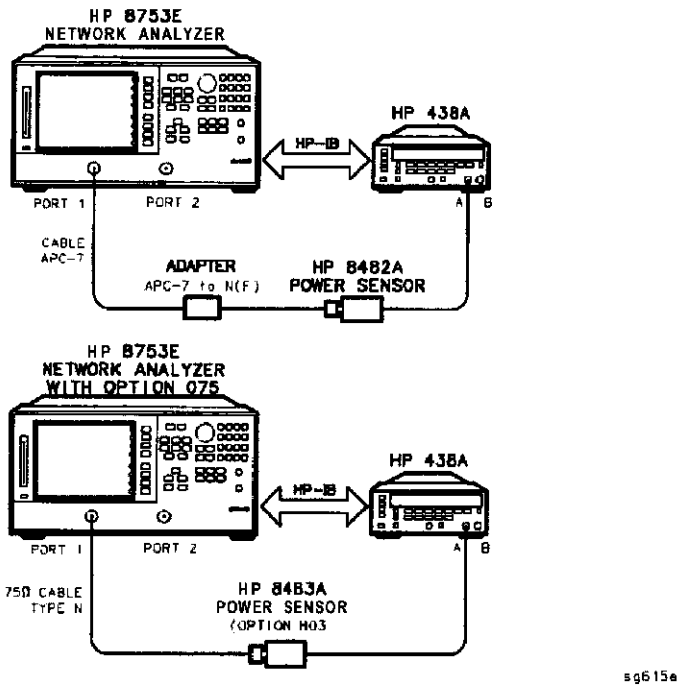


Figure 2-17. Setup for Power Meter Calibration on Test Port I

3. Press (Preset) (Start) (300) (k/m).
4. **Only for Analyzers with Option 006:** Press (Stop) (3) (G/n).
5. Press (Local) **SYSTEM CONTROLLER** .
6. Press SET ADDRESSES and POWER **MTR** until the analyzer shows the correct power meter model.

7. Press ADDRESS: **PMTR/HPIB**. The default power meter HP-IB address is 13. Make sure it is the same as your power meter HP-IB address. Otherwise, use the analyzer front panel keypad to enter the correct HP-IB address for your power meter.

8. Press (Menu) **NUMBER** of POINTS (51) (x1).

9. Press POWER PWR RANGE MAN to turn the auto power range off

---

Note The analyzer displays the **PRm** annotation, indicating that the analyzer power range is set to MANUAL.

---

10. Press PORT POWER to uncouple the test port output power

11. Press (Cal) **PWRMTR** CAL .

12. Press LOSS/SENSE LISTS **CAL FACTOR** SENSOR A . Refer to the back of the power sensor to locate the different calibration factor values along with their corresponding frequencies.

Note The analyzer's calibration factor sensor table can hold a ***maximum*** of 12 calibration factor data points.

The following **softkeys** are included in the sensor calibration factor entries menu:

SEGMENT	press to select a point where you can use the front panel knob or entry keys to enter a value.
EDIT	press to edit or change a previously entered value.
DELETE	press to delete a point from the sensor calibration factor table.
ADD	select this key to add a point into the sensor calibration factor table.
CLEAR LIST	select this key to erase the entire sensor calibration factor table.
DONE	select this key when done entering points to the sensor calibration factor table.

As an example, the following are the keystrokes for entering the first two calibration factor data points for the HP 8482A power sensor (assuming CF% = 96.4 at 100 kHz and CF% = 98.4 at 300 kHz):

a. From the sensor calibration factor entries menu, press **ADD**.

b. Press FREQUENCY (100) (k/m). If you make an entry error, press (←) and re-enter the correct value again.

c. Press **CAL FACTOR** (96.4) (x1).

d. Press **DONE** to terminate the first calibration factor data point entry.

e. To enter the second cal factor data point, press ADD.

f. Press FREQUENCY (300) (k/m).

g. Press CAL FACTOR (98.4) (x1).

h. To terminate the second calibration factor data point entry, press **DONE**.

i. Press SEGMENT and use the front panel knob to scroll through the sensor calibration factors table. Check to be sure all values are entered correctly. If you spot an error, use the front panel knob to point to the data point you want to modify and press EDIT.

13. Press the appropriate **softkeys** to create a power sensor calibration factors table.

14. Press **DONE** to exit the sensor calibration factor entries menu.

15. Press **RETURN ONE** SWEEP TAKE **CAL** SWEEP to start the power meter calibration.

    Wait until the analyzer finishes the sweep, then continue with this procedure.

Note The analyzer displays the PC annotation, indicating the power meter calibration is done and the error correction is active.

Test Port 2 Input Frequency Response from 300 kHz to 3 GHz

16. Connect the equipment as shown in Figure 2-18.

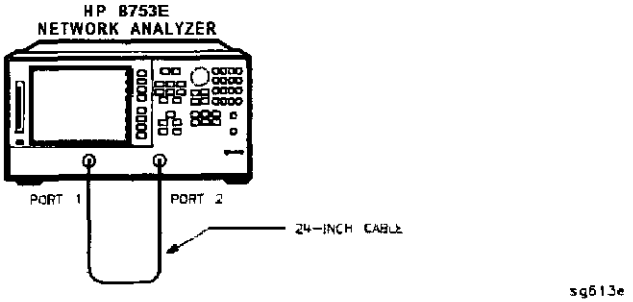


Figure 2-18. Test Port 2 Input Frequency Response Test Setup

17. Press (Meas) INPUT PORTS **B**.

18. Press (Scale Ref) **SCALE/DIV** (1) (x1).

19. Press (Marker) MARKER 1 (Marker Fctn) MKR **SEARCH SEARCH:MIN** to put marker 1 at the minimum magnitude location of the trace.

20. Press (Marker) MARKER 2 (Marker Fctn) MKR SEARCH **SEARCH:MAX** to position marker 2 at the maximum magnitude location of the trace.

21. Write the marker 1 or marker 2 value (which appears on the analyzer display), whichever has the larger absolute magnitude, in the "Performance Test Record."

Power Meter Calibration on Port 2 from 300 kHz to 3 GHz

22. Connect the equipment as shown Figure 2-19.

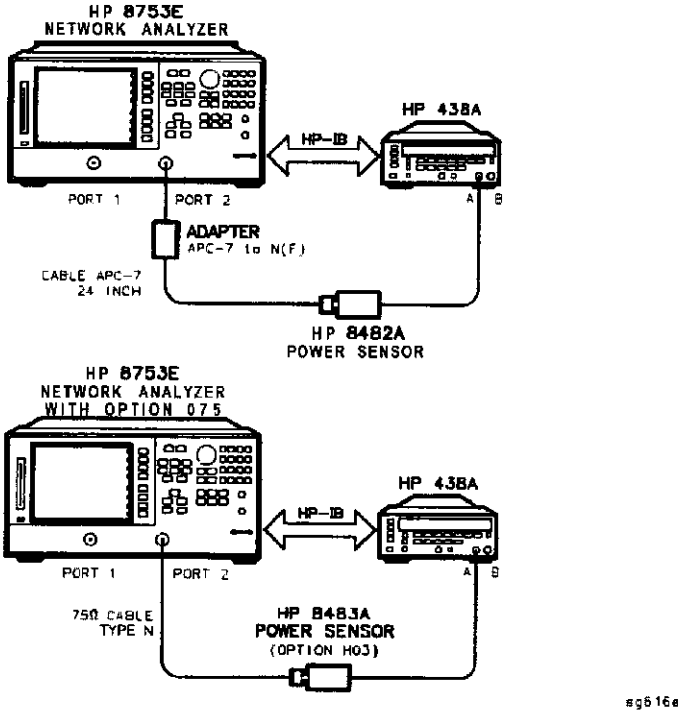


Figure 2-19. Setup for Power Meter Calibration onTest Port 2

23. Press (Meas) **INPUT** PORTS **TESTPORT** 2.

24. Press [call **PWRMTR CAL** SWEEP TAKE CAL SWEEP to start the power meter calibration for test port 2.

25. When the analyzer displays the message POWER METER CALIBRATION SWEEP DONE, connect the equipment as shown as in Figure 2-20.

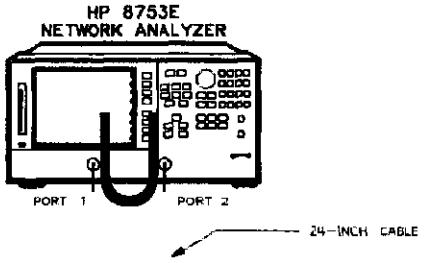


Figure 2-20. **Test** Port 1 Input Frequency Response **Test** Setup

Test Port 1 Input Frequency Response from 300 kHz to 3 GHz

26. Press (Meas) **INPUT PORTS** A.
27. Press (Marker) **MARKER 1** (Marker Fctn) **MKR SEARCH SEARCH:MIN** .
28. Press (Search) **MARKER 2** (Marker Fctn) **:MAXSEARCH** .
29. Write the marker 1 or marker 2 reading, whichever has the larger absolute magnitude, in the "Performance Test Record."
30. This completes the "Test Port Input Frequency Response" procedure if your analyzer does not have Option 006. Otherwise continue with the next sections.

Power Meter Calibration for Test Port 2 from 3 GHz to 6 GHz

31. Replace the power sensor with the HP 8481A, and then setup the power meter:
    - If the power meter is an HP 438A, press (LCL).
    - If the power meter is an HP 437B, press [PRESET/LOCAL].
    - If the power meter is an HP 436A, cycle the line power.
32. Connect the equipment as shown in Figure 2-21.

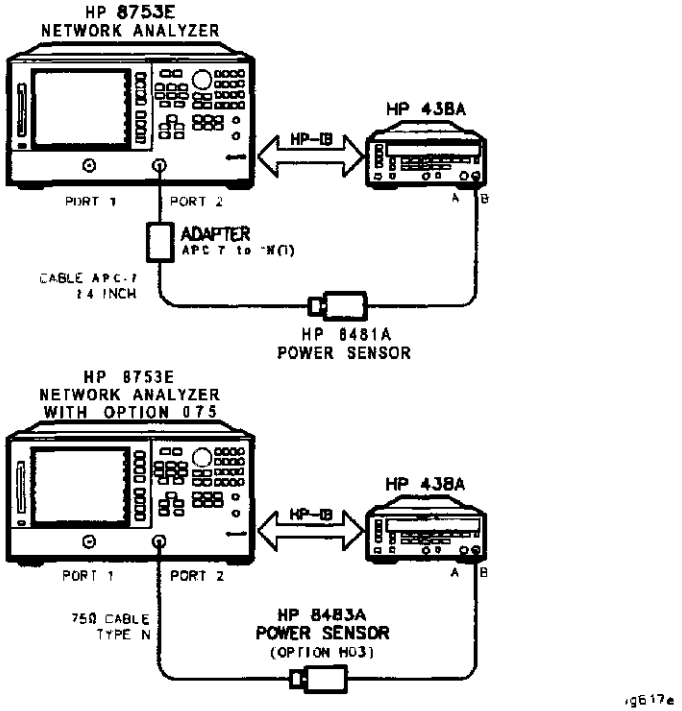


Figure 2-21. Setup for Power Meter Calibration on Test Port 2

33. Press (Start) (3) (G/n) (Stop) (6) (G/n).

34. Press (Cal) **PWRMTR** CAL.

35. Press **LOSS/SENSR** LISTS CAL FACTOR SENSOR **B** . Repeat step 12 to build a calibration factor sensor table for the HP 8481A power sensor.

36. Press DONE to exit the sensor calibration factor entries menu.

37. To select the HP 8481A power sensor, press USE SENSOR **B**.

38. Press **RETURN TAKE** CAL SWEEP to start the power meter calibration.

Test Port 1 Input Frequency Response from 3 GHz to 6 GHz

39. When the analyzer finishes the calibration sweep, connect the equipment as shown in Figure 2-22.

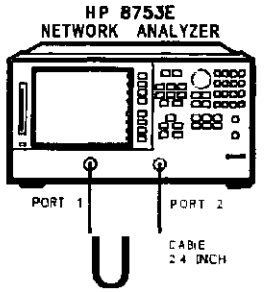


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Figure 2-22. Setup for Test Port 1 Input Frequency Response

40. Press (Meas) INPUT **PORTS A**.

41. Press (Marker) MARKER 1 (Marker Fctn) **MKR SEARCH SEARCH:MIN** to put marker 1 at the minimum magnitude location of the trace.

42. Press (Marker) MARKER 2 (Marker Fctn) **MKR** SEARCH **SEARCH:MAX** to position marker 2 at the maximum magnitude loeation of the trace.

43. Write the marker 1 or marker 2 reading, whichever has the largest absolute magnitude, in the "Performance Test Record."

Power Meter Calibration on Test Port 1 from 3 GHz to 6 GHz

44. Connect the equipment as shown in Figure 2-23.

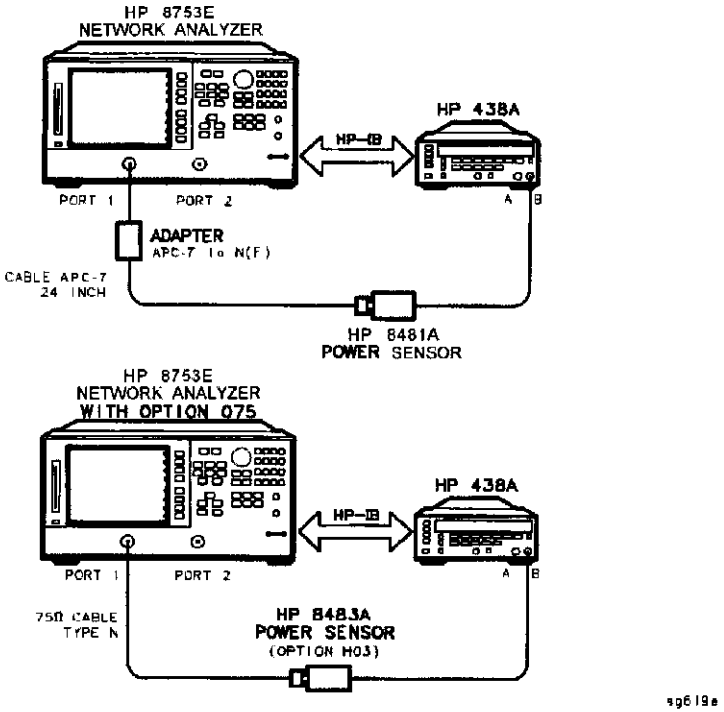

Figure Z-23. Setup for Power Meter Calibration on Test Port 1

45. Press (Meas) **INPUT PORTS TESTPORT 1**.

46. Press (Cal) **PWRMTR ONE** SWEEP TAKE CAL SWEEP to start the power meter calibration for output test port 1.

Test Port 2 Input Frequency Response from 3 GHz to 6 GHz

47. When the analyzer displays the message POWER METER CALIBRATION SWEEP DONE, connect the equipment as shown as in Figure 2-24.

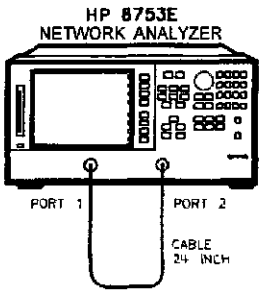

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Figure 2-24. Test Port 2 Input Frequency Response Test Setup

48. Press (Meas) INPUT PORTS B.

49. Press (Marker) MARKER 1 (Marker Fctn) MKR SEARCH SEARCH:MIN.

50. Press (Marker) MARKER 2 (Marker Fctn) MKR SEARCH SEARCH: MAX.

51. Write the marker 1 or marker 2 reading, whichever has the largest magnitude, in the "Performance Test Record."

In Case of Difficulty

1. Be sure you have used the correct power sensor for the frequency range.
2. Verify that the calibration factors that you have entered for the power sensors are correct.
3. Repeat this test with a "known good" through cable.

8. Test Port Crosstalk

Specifications

Frequency Range	Crosstalk[1]
300 kHz to 3 GHz	100 dB
3 GHz to 6 GHz[2]	90 dB

1 At 25° C ±5° C

2 Only for analyzers with Option 006 – 30 kHz to 6 GHz range.

Required Equipment for 508 Analyzers

Calibration Kit, 7-mm ..... HP 85031B
Cable, APC-7 24-inch ..... HP P/N 8120-4779

Required Equipment for 753 Analyzers

Calibration Kit, 750, Type-N ..... HP 85036B

Analyzer warmup time: **1 hour**

Perform this test to verify the signal leakage between the analyzer's test ports.

1. Connect the equipment as shown in Figure 2-25.

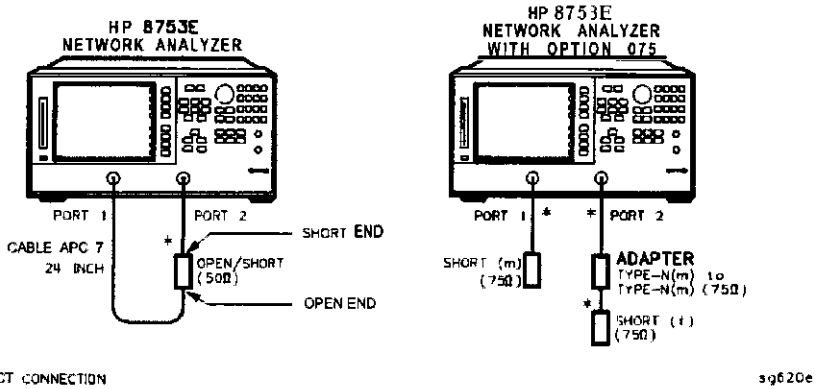

Figure 2-25. Test Port Crosstalk Test Setup

2. Press (Preset) (Menu) POWER (10) (x1).

3. Press (Avg) IF BW (10) (x1).

Crosstalk to Test Port 2 from 300 kHz to 3 GHz

4. Press (Start) (300) (k/m) (Stop) (3) (G/n).

5. Press (Meas) Trans: FWD S21 (B/R).

6. Press (Scale Ref) REFERENCE VALUE (-100) (x1).

7. Press (Menu) TRIGGER MENU SINGLE.

8. Press (Marker Fctn) MKR SEARCH SEARCH: MAX.

9. Write the marker value (which appears on the analyzer display) in the "Performance Test Record."

Crosstalk to Test Port 1 from 300 kHz to 3 GHz

10. Press (Meas) Trans: REV S12 (A/R).

11. Press (Menu) TRIGGER MENU SINGLE.

12. Press (Marker Fctn) MKR SEARCH SEARCH: MAX.

13. Write the marker value (which appears on the analyzer display) in the "Performance Test Record."

14. This completes the "Test Port Crosstalk" performance test if your analyzer does not have Option 006. Otherwise, proceed to the next section.

Crosstalk to Test Port 1 from 3 GHz to 6 GHz

15. Press (Start) (3) (G/n) (Stop) (6) (G/n).

16. Press (Menu) TRIGGER MENU SINGLE.

17. Press (Marker Fctn) MKR SEARCH SEARCH: MAX.

18. Write the marker value (which appears on the analyzer display) in the "Performance Test Record."

Crosstalk to Test Port 2 from 3 GHz to 6 GHz

1. Press (Meas) Trans: FWD S21 (B/R).
2. Press (Menu) TRIGGER MENU SINGLE.
3. Press (Marker Fctn) MKR SEARCH SEARCH: MAX.
4. Write the marker value (which appears on the analyzer display) in the "Performance Test Record."

In Case of Difficulty

1. Remove the instrument top cover. Using an 8 lb-inch torque wrench, verify that *all* semirigid cables connected to the sampler/mixer assemblies are tight. In addition, tighten any loose screws on the sampler/mixer assemblies (A4/5/6) and the pulse generator assembly (A7).
2. Remove the instrument bottom cover. Refer to Figure 2-26. Verify that cables W1, W31 and W32 are tight.
3. Repeat this test.

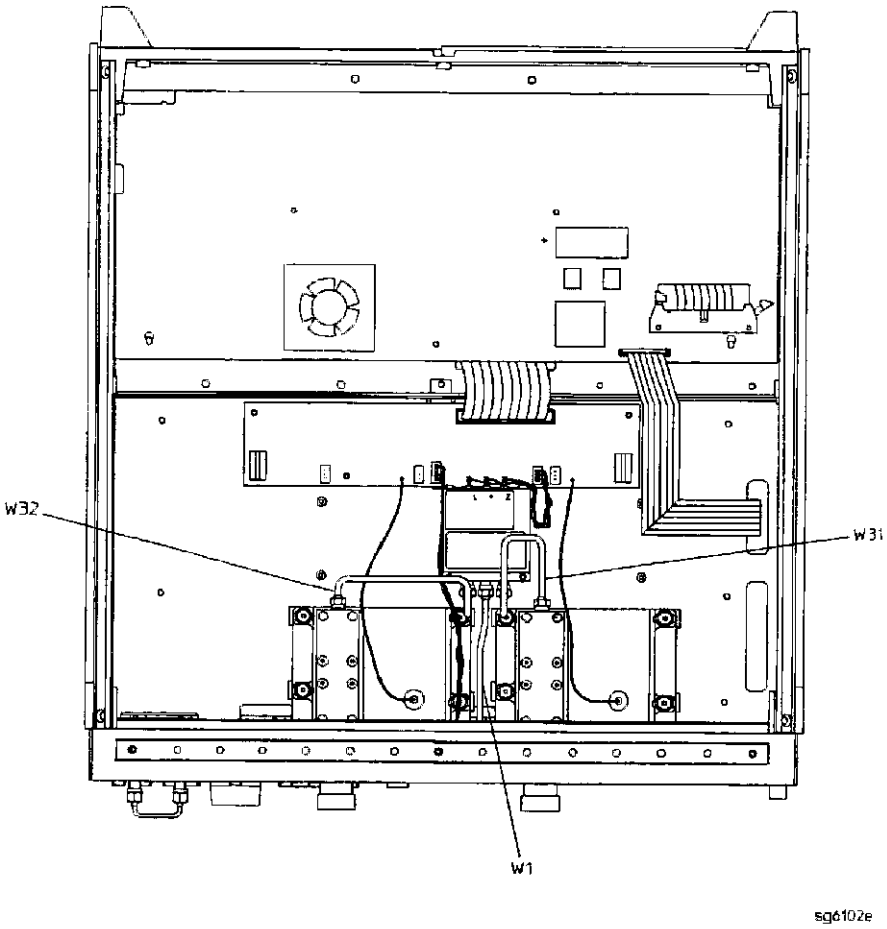

Figure 2-26. HP 87533 Bottom View

9. Calibration Coefficients

Specifications

Uncorrected[1] Error Terms	Frequency Range		
	300 kHz to 1.3 GHz	1.3 GHz to 3 GHz	3 GHz to 6 GHz[2]
Directivity	35 dB	30 dB	25 dB
Source Match	16 dB	16 dB	14 dB
Load Match	18 dB	16 dB	14 dB
Transmission Tracking	±1.5 dB	±1.5 dB	±2.5 dB
Reflection Tracking	±1.5 dB	±1.5 dB	±2.5 dB

1 At 25° ±5° C, with less than 1° C deviation from the measurement calibration temperature

2 Only for analyzers with Option 006 – 30 kHz to 6 GHz range.

Equipment Required for 50 Ohm Analyzers

Calibration Kit, 7-mm	HP 85031B
Cable, APC-7, 24-inch	HP P/N 8120-4779

Equipment Required for 75 Ohm Analyzers

Calibration Kit, Type-N	HP 85036B
Cable, Type-N, 24-inch	HP P/N 8120-4781

***Analyzer warmup time:* 30 minutes**

Perform this procedure to verify the analyzer uncorrected test port characteristics.

Note The crosstalk calibration coefficients are omitted in this procedure. They are covered in the "Test Port Crosstalk" performance test.

First Full 2-Port Calibration

1. Connect the equipment as shown in Figure 2-27.

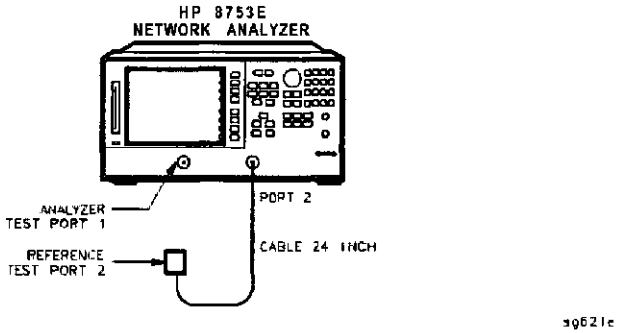

Figure 2-27. First Full Z-Port Calibration Test Setup

2. Press (Preset) (Start) (300) (k/m).
3. Press (Cal) CAL KIT SELECT CAL KIT CAL **KIT:7mm RETURN RETURN CALIBRATE MENU** FULL **2-PORT**.
4. Press ISOLATION OMIT **ISOLATION** .
5. Connect the "open" end of the open/short combination (supplied in the calibration kit) to analyzer test port 1.
6. Press **REFLECTION FORWARD:OPEN**.
7. Connect the "short" end of the open/short combination to analyzer test port 1.
8. Press **FORWARD:SHORT**.
9. Replace the open/short combination with the 50 ohm termination (supplied in the calibration kit).
10. Press FORWARD:**LOAD**.
11. Connect the "open" end of the open/short combination to the reference test port 2.

12. Press REVERSE: OPEN.

13. Connect the "short" end of the open/short combination to the reference test port 2.

14. Press REVERSE: SHORT.

15. Connect the 50 ohm termination to the reference test port 2.

16. Press REVERSE: **LOAD**.

17. **When the analyzer displays** PRESS **'DONE'** IF FINISHED WITH **STD(s)**, press STANDARDS DONE.

    Wait for the message COMPUTING CAL COEFFICIENTS to disappear from the analyzer display before proceeding to the next step.

18. Connect the equipment as shown in Figure 2-28.

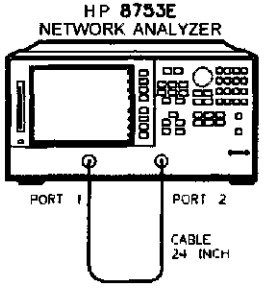

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Figure 2-28. Transmission Calibration Test Setup

19. Press TRANSMISSION **DO BOTH FWD** + REV.

20. Press DONE Z-PORT CAL.

Directivity (Forward) Calibration Coefficient

21. Press (System) SERVICE MENU TESTS (32) (x1) EXECUTE TEST.
22. When the analyzer finishes the test, press (Marker).
23. Using the front panel knob, locate the maximum value of the data trace for the 300 kHz to 1.3 GHz frequency range.
24. Write the maximum value in the "Performance Test Record."
25. Repeat the previous two steps for the other frequency range(s) listed on the "Performance Test Record."

Source Match (Forward) Calibration Coefficient

26. Press (System) SERVICE MENU TESTS 133) (x1) EXECUTE TEST.
27. When the analyzer finishes the test, repeat steps 22 through 26.

Transmission Tracking (Forward) Calibration Coefficient

28. Press (System) SERVICE MENU TESTS (37) (x1) EXECUTE TEST.
29. When the analyzer finishes the test, repeat steps 22 through 25.

Reflection Tracking (Forward) Calibration Coefficient

30. Press (System) SERVICE MENU TESTS (341 (x1) EXECUTE TEST.
31. When the analyzer finishes the test, repeat steps 22 through 25.

Load Match (Reverse) Calibration Coefficient

32. Press (System) SERVICE MENU TESTS (42) (xl) EXECUTE TEST.
33. When the analyzer finishes the test, repeat steps 22 through 25.

Transmission Tracking (Reverse) Calibration Coefficient

34. Press System SERVICE MENU TESTS 43 [xl) EXECUTE TEST.

35. When the analyzer finishes the test, repeat steps 22 through 25.

Second Full 2-Port Calibration

36. Connect the equipment as shown in Figure 2-29.

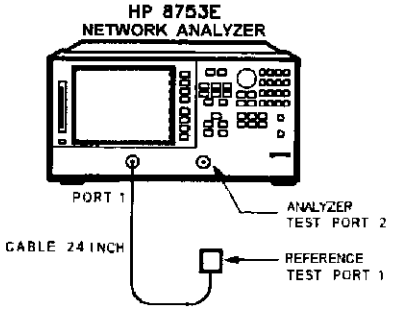

Figure 2-29. Second Full 2-Port Calibration Test Setup

37. Press Preset Start 300 k/m.

38. Press Cal CAL KIT SELECT CAL KIT CAL KIT 7mm RETURN RETURN CALIBRATE MENU FULL 2-PORT.

39. Press ISOLATION OMIT ISOLATION .

40. Connect the "open" end of the open/short combination (supplied in the calibration kit) to reference test port 1.

41. Press REFLECTION FORWARD:OPEN.

42. Connect the "short" end of the open/short combination to reference test port 1.

43. Press FORWARD:SHORT.

44. Replace the open/short combination with the 50 ohm termination (supplied in the calibration kit).

45. Press FORWARD: **LOAD**.

46. Connect the "open" end of the open/short combination to the analyzer test port 2.

47. Press REVERSE : **OPEN**.

48. Connect the "short" end of the open/short combination to the analyzer test port 2.

49. Press REVERSE: SHORT.

50. Connect the 50 ohm termination to the analyzer test port 2.

51. Press REVERSE: **LOAD**.

52. When the analyzer displays PRESS'**DONE**' IF FINISHED WITH STD(**s**), press STANDARDS DONE.

    Wait for the message COMPUTING CAL COEFFICIENTS to disappear from the analyzer display before proceeding to the next step.

53. Connect the equipment as shown in Figure 2-30.

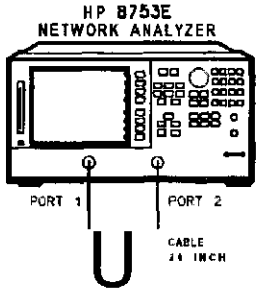

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Figure 2-30. Transmission Calibration Test Setup

54. Press TRANSMISSION **DO BOTH FWD** + REV .

55. Press DONE %-PORT CAL .

Load Match (Forward) Calibration Coefficient

56. Press (System) SERVICE MENU TESTS (36) (x1) EXECUTE TEST.

57. When the test is done, press (Marker) MARKER 1.

58. Using the front panel knob, locate the maximum value of the data trace for the 300 kHz to 1.3 GHz frequency range.

59. Write the maximum value on the "Performance Test Record."

60. Repeat the previous three steps for the other frequency range(s) listed on the "Performance Test Record."

Directivity (Reverse) Calibration Coefficient

61. Press (System) SERVICE MENU TESTS (38) (x1) EXECUTE TEST.

62. When the analyzer finishes the test, repeat steps 57 through 60.

Source Match (Reverse) Calibration Coefficient

63. Press (System) SERVICE MENU TESTS (39) (x1). At the prompt, press EXECUTE TEST.

64. When the analyzer finishes the test, repeat steps 57 through 60.

Reflection Tracking (Reverse) Calibration Coefficient

65. Press (System) SERVICE MENU TESTS (40) [x1] EXECUTE TEST.

66. When the analyzer finishes the test, repeat steps 57 through 60.

10. System Trace Noise (Only for Analyzers without Option 006)

Frequency Range	Ratio	System Trace Noise (Magnitude[1])	System Trace Noise (Phase[1])
30 kHz to 3 GHz	A/R	<0.006 dB rms	<0.038° rms
30 kHz to 3 GHz	B/R	<0.006 dB rms	<0.038° rms

1 At + 5 dBm into test port, 3 kHz IF bandwidth, and CW sweep

Required Equipment for 50 Ohm Analyzers

Cable, APC-7, 24-inch HP P/N 8120-4779

Required Equipment for 75 Ohm Analyzers

Cable, 750, Type-N 24-inch .HP P/N 8120-2408

Analyzer warmup time: 1 hour

Perform this test to measure the system trace noise at a designated frequency in both the A/R and B/R ratioed measurements.

1. Connect the equipment as shown in Figure 2-31.

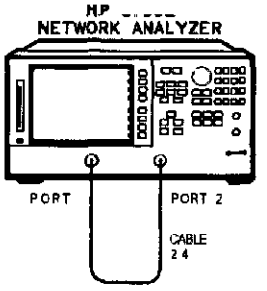

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Figure 2-31. System Trace Noise Test Setup

2. Press [Preset] [MENU][POWER][5](x1).

Press CW NUMBER of (x1).

4. Press (Marker Fctn) MARKER **MODE MENU** STATS **ON** to activate the instrument's statistic feature.

System Trace Noise for A/R Magnitude

5. Press (Meas) **Trans:** REV **S12** CA/R) .

6. Press (Menu) TRIGGER MENU **NUMBER** of GROUPS (5) (xl

7. When the analyzer displays the "Hld" annotation, press (Scale Ref) **AUTO** SCALE

8. Write the s.dev (standard deviation) value, which appears on the analyzer display, on the "Performance Test Record. "

System Trace Noise for A/R Phase

9. Press (Format) PHASE,

10. Press (Menu) TRIGGER MENU NUMBER of GROUPS (5) (x1).

11. When the analyzer finishes the number of sweeps, press (Scale Ref) **AUTO** SCALE.

12. Write the s.dev value on the "Performance Test Record."

System Trace Noise for B/R Magnitude

13. Press (Meas) **Trans:** FWD **S21 (B/R).**

14. Press (Menu) TRIGGER MENU **NUMBER** of GROUPS (5) (x1).

15. When the analyzer finishes the number of sweeps, press (Scale Ref) **AUTO** SCALE.

16. Write the s.dev value on the "Performance Test Record."

System Trace Noise for B/R Phase

17. Press [Format] PHASE.

18. Press [Menu] TRIGGER MENU NUMBER of GROUPS [5] [x1].

19. When the analyzer finishes the number of sweeps, press [Scale Ref] AUTO SCALE.

20. Write the s.dev value on the "Performance Test Record."

In Case of Difficulty

1. Perform the "ADC Offset Correction Constants" procedure, located Chapter 3, "Adjustments and Correction Constants."

2. Repeat this performance test.

3. Suspect the A10 Digital IF board assembly if the analyzer still fails the test.

11. System Trace Noise (Only for Analyzers with Option 006)

Specifications

Frequency Range	Ratio	System Trace Noise (Magnitude[1])	System Trace Noise (Phase[1])
30 kHz to 3 GHz	A/R	<0.006 dB rms	<0.038° rms
30 kHz to 3 GHz	B/R	<0.006 dB rms	<0.038° rms
3 GHz to 6 GHz	A/R	<0.010 dB rms	<0.070° rms
3 GHz to 6 GHz	B/R	<0.010 dB rms	<0.070° rms

1 At + 5 dBm into test port, 3 kHz IF bandwidth, and CW sweep

Required Equipment

Cable, APC-7, 24-inch . ... HP P/N 8120-4779

***Analyzer warmup time:* 1 hour**

Perform this test to measure the system trace noise at designated CW frequencies in both the A/R and B/R ratioed measurements.

1. Connect the equipment as shown in Figure 2-32.

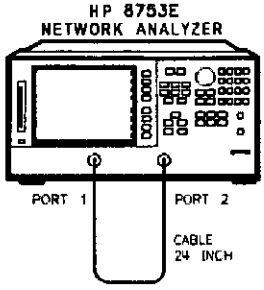

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Figure 2-32. System Trace Noise Test Setup

2. Press (Preset) (Menu) POWER (5) (x1) RETURN NUMBER of POINTS (1601) (x1).

3. Press (Marker Fctn), MARKER **MODE MENU** STATS ON to activate the instrument's statistic feature.

System Trace Noise for A/R Magnitude from 30 kHz to 3 GHz

4. Press (Meas) **Trans: REV S12 (A/R)**.

5. Press (Menu) CW **FREQ** (3) (G/n) **TRIGGER MENU NUMBER** of **GROUPS** (5) (x1).

6. When the analyzer finishes the number of sweeps, press (Scale Ref) **AUTO** SCALE.

7. Write the s.dev (standard deviation) value shown, which appears on the analyzer display, on the "Performance Test Record."

System Trace Noise for A/R Magnitude from 3 GHz to 6 GHz

8. Press [Menu) CW **FREQ** (6) (G/n) TRIGGER MENU **NUMBER** af **GROUPS** (5) (x1).

9. When the analyzer finishes the number of sweeps, press (Scale Ref) **AUTO** SCALE.

10. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record."

System Trace Noise for A/R Phase from 3 GHz to 6 GHz

11. Press (Format) PHASE.

12. Press (Menu) TRIGGER **MENU NUMBER** of **GROUPS** (5) (x1).

13. When the analyzer finishes the number of sweeps, press (Scale Ref) **AUTO** SCALE.

14. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record "

System Trace Noise for A/R Phase from 30kHz to 3 GHz

15. Press (Menu) CW FREQ (3) (G/n) TBIGGEB MENU NUMBER of CROUPS (5) (x1).
16. When the analyzer finishes the number of sweeps, press (Scale Ref) AUTO SCALE.
17. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record"

System Trace Noise for B/R Magnitude from 30kHz to 3 GHz

18. Press (Meas) Trans : FWD S21 (B/R) (Menu) TBIGGEB MENU NUMBER of GROUPS (5) (x1).
19. When the analyzer finishes the number of sweeps, press (Scale Ref) AUTO SCALE.
20. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record."

System Trace Noise for B/R Magnitude from 3GHz to 6 GHz

21. Press (Menu) CW FREQ (6) (G/n) TRIGGER MENU NUMBER of GROUPS (5) (x1).
22. When the analyzer finishes the number of sweeps, press (Scale Ref) AUTO SCALE.
23. Write the s dev value, which appears on the analyzer display, on the " Performance Test Record. "

System Trace Noise for B/R Phase from 3GHz to 6 GHz

24. Press (Format) PHASE (Menu) TRIGGER MENU NUMBER of GROUPS (5) (x1).
25. When the analyzer finishes the number of sweeps, press (Scale Ref) AUTO SCALE.
26. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record. "

System Trace Noise for B/R Phase from 30 kHz to 3 GHz

27. Press (Menu) CW FREQ (3) (G/n) TRIGGER MENU NUMBER of GROUPS (5) (x1).
28. When the analyzer finishes the number of sweeps, press (Scale Ref) AUTO SCALE.
29. Write the s.dev value, which appears on the analyzer display, on the "Performance Test Record."

In Case of Difficulty

1. Perform the "ADC Offset Correction Constants" procedure, located in Chapter 3, "Adjustments and Correction Constants."
2. Repeat this performance test.
3. Suspect the A10 Digital IF board assembly if the analyzer still fails the test.

12. Test Port Input Impedance

Specifications

Frequency Range	Test Port Input	Return Loss
300 kHz to 1.3 GHz	Port 1	≥18 dB
1.3 GHz to 3 GHz	Port 1	≥16 dB
3 GHz to 6 GHz	Port 1	≥14 dB
300 kHz to 1.3 GHz	Port 2	≥18 dB
1.3 GHz to 3 GHz	Port 2	≥16 dB
3 GHz to 6 GHz	Port 2	≥14 dB

Required Equipment for 50Ω Analyzers

Cable, APC-7, 24-inch ..... HP P/N 8120-4779
Calibration Kit, 7-mm ..... HP 85031B

Required Equipment for 75Ω Analyzers

Cable, 75Ω, Type-N, 24-inch ..... HP P/N 8120-2408
Calibration Kit, 7561, Type-N ..... HP 85036B

Analyzer warmup time: **1 hour**

Perform this test to measure the return loss of each input test port.

1. Connect the equipment as shown in Figure 2-33.

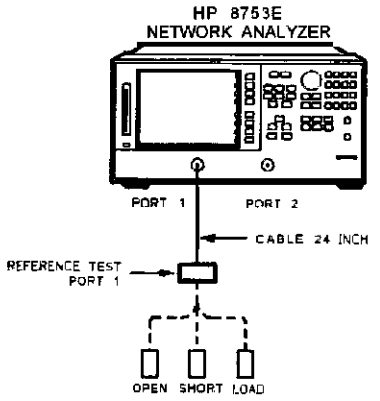


Figure 2-33. S11 1-Port CM Test Setup

2. Press (Preset) (Menu) NUMBER of POINTS (1601) (x1).
3. Press (Start) (300) (k/m).
4. Press (Cal) CAL KIT SELECT CAL KIT and select the appropriate calibration kit:
   - If your analyzer is 500, press CAL KIT: 7mm.
   - If your analyzer is 758, press CAL KIT: N 75Ω.
5. Press RETURN RETURN CALIBRATE MENU S11 1-PORT.
6. Connect an open to reference test port 1, as shown in Figure 2-33.
7. Press FORWARD: OPEN.

a. When the analyzer displays the prompt CONNECT STD THEN PRESS KEY TO MEASURE, connect a short to reference test port 1.

9. Press FORWARD: SHORT.
10. At the prompt, connect a load to reference test port 1.

11. Press FORWARD : LOAD .

12. When the analyzer displays 'DONE' IF FINISHED WITH CAL, press DONE I-PORT CAL.

13. Press [Save/Recall) SAVE STATE.

14. Connect the equipment as shown in Figure 2-34.

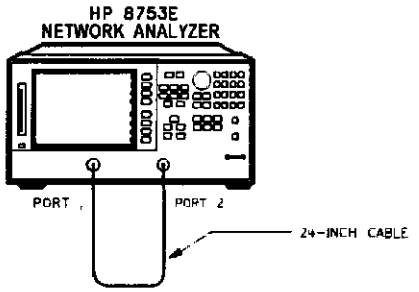


Figure 2-34. **Test** Port 2 Input Impedance **Test** Setup

15. Press (Marker) to turn the analyzer's marker 1 on. Use the front panel knob to locate the maximum value of the data trace for each of the frequency ranges listed in the "Performance Test Record. "

16. Write these maximum **values** on the 'Performance Test Record."

17. Connect the equipment as shown in Figure 2-35.

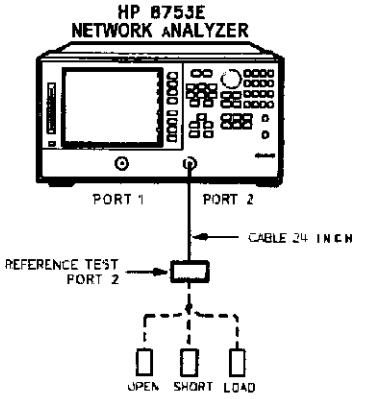


Figure 2-35. **S22** 1-Port **Cal Test** Setup

18. Press (Cal) CALIBRATE MENU**S22 1-PORT**.
19. At the prompt, connect an open to reference test port 2, as shown in Figure 2-35.
20. Press REVERSE: **OPEN**.
21. When the analyzer displays the prompt CONNECT STD THEN PRESS KEY TO MEASURE, connect a short to reference test port 2.
22. Press REVERSE: **SHORT**.
23. At the prompt, connect a load to reference test port 2.
24. Press **REVERSE: LOAD**.
25. When the analyzer displays 'DONE' IF FINISHED WITH CAL, press **DONE** I-PORT CAL.
26. Press (Save/Recall) SAVE STATE to save the I-Port calibration.
27. Connect the equipment as shown in Figure 2-36.

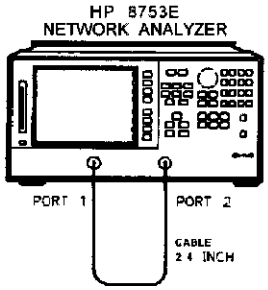


Figure 2-36. Test Port 1 Input Impedance Test Setup

28. Press (Marker) to activate the analyzer's marker 1. Use the front panel knob to locate the maximum value of the data trace for each of the frequency ranges listed in the "Performance Test Record."

29. Write the maximum values on the "Performance Test Record."

In Case of Difficulty

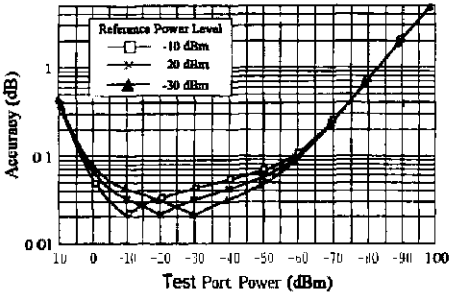
1. Suspect the A10 digital IF **board assembly** if the analyzer fails ***both*** test port tests.

2. Refer to Chapter 8, "Receiver Troubleshooting," for more troubleshooting information.

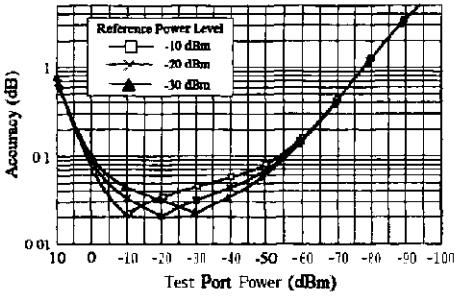
13. Test Port Receiver Magnitude Dynamic Accuracy

Specifications

HP8753E Magnitude Dynamic Accuracy 0.3 to3000 MHz



HP8753E Magnitude Dynamic Accuracy 3-6 GHz



Required Equipment

Power Meter	HP 436A/437B/438A
Power Sensor	HP 8482A
Step Attenuator, 110 dB	HP 8496A Option 001, H18
(See notes on the following page.)	
Adapter (2), APC-7 to Type-N (f)	HP 11524A
Adapter, Type-N (f) to Type-N (f)	HP P/N 1250-0777
Cable (3), 50Ohm Type-N, 24-inch	8120-4781
Cable, HP-IB	HP 10833A
Diskette, 3.5 inch	any
Calibration Kit, Type-N, 50 Ω	HP 85032B

Additional Required Equipment for 753 Analyzers

Minimum Loss Pad (2), 50Ω to 75Ω	HP 11852B

Analyzer warmup time: **1 hour**

Note

The HP 8496A step attenuator (Option 001, H18) comes with a special calibration that supports the measurement uncertainties expressed in the test record for this performance test.

The special calibration consists of two measurements The first is a measurement of the attenuation at each step. The data reported for this measurement have the following uncertainties:

- f0 006 dB from 0 to 40 dB
- 10.015 dB from >40 to 80 dB
- ±0.025 dB from >80 to 90 dB
- ±0.05 dB >90 dB

The second calibration measurement characterizes match stability between attenuator settings for each attenuator port. The vector difference of S_{11} or (S_{22}) between the reference attenuation step and all the other steps is measured. The magnitude of this difference is certified to be ~0.0316 (>30 dB).

Note

The HP 8496A used for this test will have known attenuator errors for attenuations up to 100 dB using a test frequency of 30 MHz. The attenuation used as a reference is 0 dB. If the available calibration data is not expressed as attenuation errors, it can be converted to such a form by the following equation:

(actual attenuation) − (expected attenuation) = attenuator error

Actual attenuation values that are greater than the expected attenuation values will result in positive errors. Actual attenuation values that are less than the expected attenuation values will result in negative errors.

Initial Calculations

1. Fill in the attenuator error values (referenced to 0 dB attenuation) in Table 2-1 by referring to the calibration data for the HP 8496A step-attenuator. Refer to the note on the previous page.
   a. Find the column in the HP 8496A attenuation error table that pertains to the attenuation errors for 30 MHz.
   b. Starting with the " 10 dB" step in this column, write down the value in the corresponding space in Table 2-1 for column "B. " This value should be placed in the row for the 10 dB HP 8496A setting.
   c. Continue transferring the remaining values of the HP 84966 attenuation errors to column "B" in Table 2- 1.
2. In Table 2-1, transfer the 10 dB error value located within the parenthesis in column "B" to each space column "C. "

Table 2-1. Magnitude Dynamic Accuracy Calculations

A	B	C	D (B – C)	E	F (E – D)
8496A Attn. (dB)	Attn. Error (ref 0 dB)	10 dB Error Value	Attn. Error (ref 10 dB)	Expected Measurement (dBm)	Expected Measurement (corrected) (dBm)
0	0 dB	_____	_____	10	_____
10	(_____)	_____	0 dB	0	_____
20	_____	_____	_____	– 10	_____
30	_____	_____	_____	– 20	_____
40	_____	_____	_____	– 30	_____
50	_____	_____	_____	– 40	_____
60	_____	_____	_____	– 50	_____
70	_____	_____	_____	– 60	_____
80	_____	_____	_____	– 70	_____
90	_____	_____	_____	– 80	_____

3. The values in column "D" result from changing the reference attenuation of the calibration data of the HP 8496A to 10 dB.

Calculate the attenuation error values for this column by subtracting the values in column "C" from the values in column "B" (B – C = D).

4. The values in column "F" result from correcting the expected measurement value by the amount of attenuator error.

   Calculate the values in this column by subtracting the values in column "D" from the values in column "E" (E – D = F).

5. Transfer the values from column "F" in Table 2-1 to column "F" in the "Performance Test Record" for both test ports.

Power Meter Calibration

6. Zero and calibrate the power meter. (Refer to the power meter manual for details on this procedure.)
7. Connect the equipment as shown in Figure 2-37.

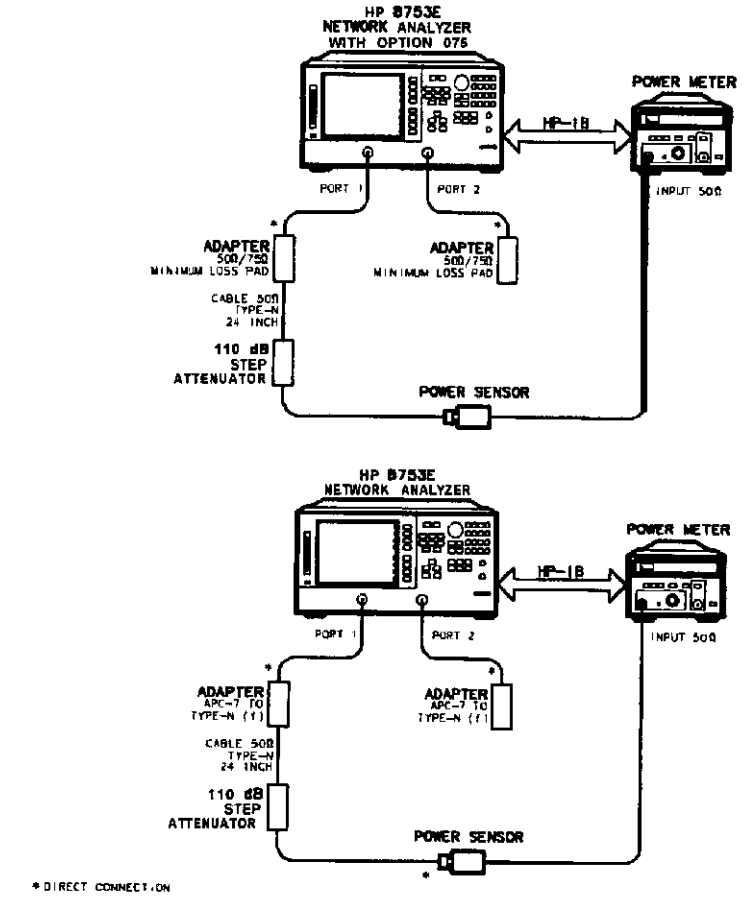


Figure 2-37. Power Meter Calibration for Magnitude Dynamic Accuracy

8. Set the HP 8496A to 10 dB.
9. Set the following analyzer parameters:

   (Preset) (Menu) CW FREQ (30) (M/μ)

   NUMBER of POINTS (51) (x1)

   POWER (−10) (x1)

   (Avg) IF BW (10) (x1)

10. Set up the HP 87533 for power meter calibration:
    a. Select the HP 87533 as the system controller:

       (Local)

       SYSTEM CONTROLLER

    b. Set the power meter's address:

       SET ADDRESSES

       ADDRESS: PWR MTR/HPIB (13) (x1)

    c. Select the appropriate power meter by pressing POWER MTR [ ] until the correct model number is displayed (HP 436A or HP 438A/437).
    d. Select the cal kit and enter the power sensor calibration data.

       (Cal) CAL KIT SELECT CAL KIT N50Ω

       (Cal) PWRMTR CAL LOSS/SENSOR LISTS CAL FACTOR SENSOR A (enter the power sensor calibration data for 30 MHz) DONE

11. Take a power meter calibration sweep.

    (Cal) PWRMTR &AL (−20) (x1)

    ONE SWEEP TAKE CAL SWEEP

12. Verify that the power meter reads approximately -20 dBm.

Adapter Removal Calibration

13. Connect the equipment as shown in the Figure Z-38:

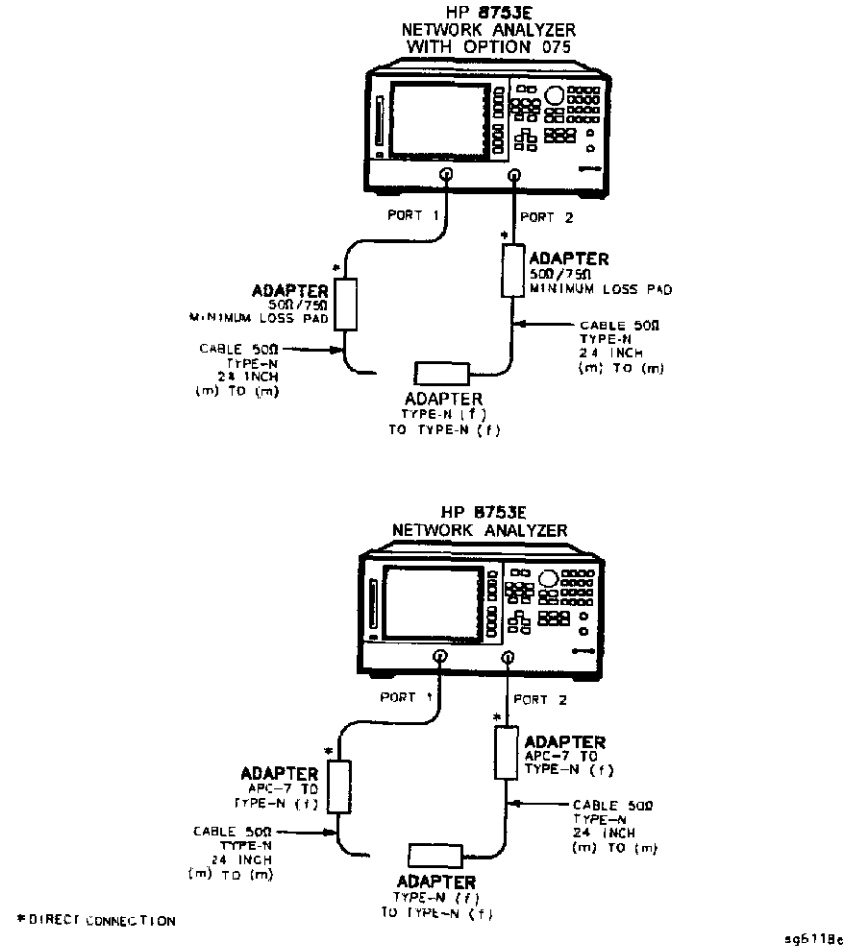


Figure 2-38. Full 2-Port Calibration with Adapter Removal

14. Perform a full 'L-port error correction with isolation.

Note When you are performing error-correction for a system that has type-N test port connectors, the softkey menus label the sex of the test port connector – *not* the calibration standard connector. For example, the label **SHORT (F)** refers to the short that will be connected to the female test port.

15. **Save** the results to disk. Name the file "PORT1."
16. Move the adapter to reference test port 1 and perform another full 2-port error correction.
17. Save the results to disk. Name the file "PORT2."
18. Press (Cal) **MORE** ADAPTER REMOVAL RECALL CAL SETS.
19. From the disk directory, choose the file "PORT1" and press RECALL &AL PORT 1.
20. When this is complete, choose the file "PORT2" and press RECALL CAL **PORT** 2.
21. When complete, press RETURN.
22. To enter the adapter delay, press ADAPTER DELAY (.110) (G/n) (default for type-N adapter 1250-1777). The analyzer display will read 110 ps.
23. Press **ADAPTER** COAX REMOVE **ADAPTER**.
24. Save the results of the new cal set.

Measure Test Port 2 Magnitude Dynamic Accuracy

25. Remove the type-N (f) to (f) adapter and connect the equipment as shown in Figure 2-39. Confirm that the step attenuator is set to 10 dB.

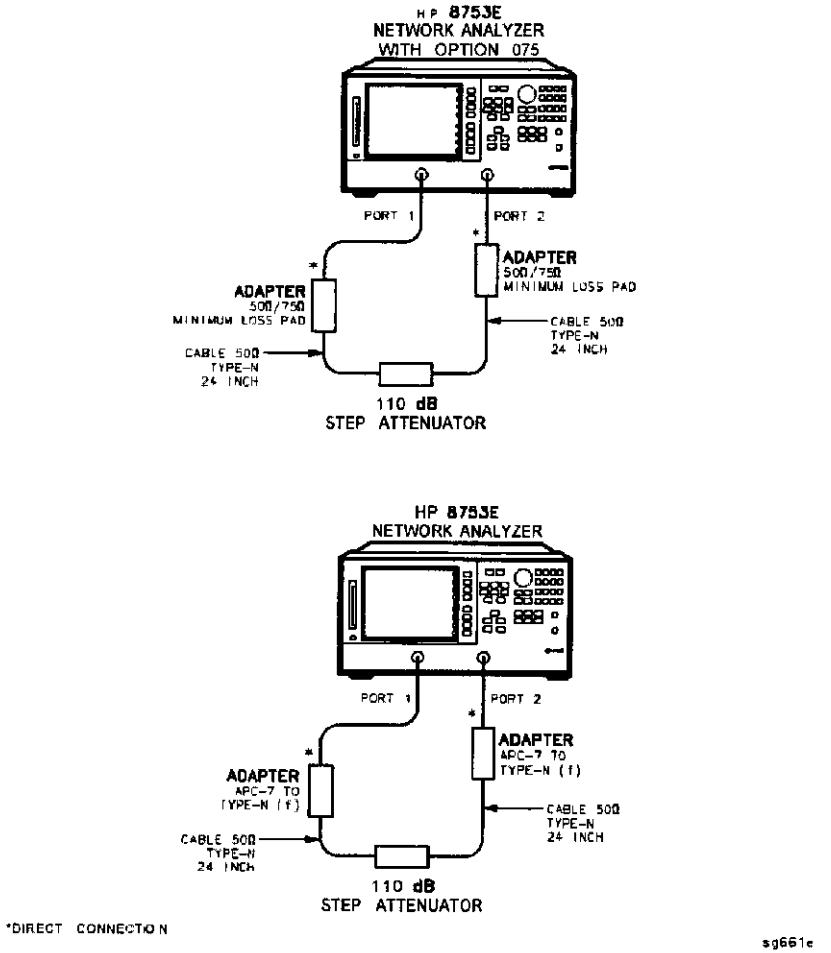


Figure 2-39. Magnitude Dynamic Accuracy Measurement

26. To set up the dynamic accuracy measurement, press the following:

(Meas) **Trans :FWD** S21 **(B/R)**

(Marker Fctn) **MKR MODE MENU** STATS **ON**

(Menu) TRIGGER MENU SINGLE

27. Wait for the sweep to finish, then press (Display) DATA → **MEM DATA/MEM** .

28. Set the step attenuator to 0 dB.

29. Press (Menu) TRIGGER MENU SINGLE.

30. Write the mean value (which appears on the analyzer's display) in the "Test Port Measurement" column of the "Performance Test Record." This column is also labeled "G."

31. Repeat steps 28 through 30 for each setting of the step attenuator.

32. Calculate dynamic accuracy for each step by using the formula $|G - F|$. Place these values in the appropriate column of the "Performance Test Record."

Measure Test Port 1 Magnitude Dynamic Accuracy

33. Set the step attenuator to 10 dB.

34. To set up the dynamic accuracy measurement, press the following:

    (Meas) **Trans:REV S12 (A/R)**

    (Display) DATA

    (Menu) **TRIGGER** MENU SINGLE

35. Wait for the sweep to finish, then press (Display) DATA → MEM **DATA/MEM**.

36. Set the step attenuator to 0 dB.

37. Press (Menu) TRIGGER **MENU SINGLE**.

38. Write the mean value (which appears on the analyzer's display) in the "Test Port Measurement" column of the "Performance Test Record." This column is also labeled "G."

39. Repeat steps 36 through 38 for each setting of the step attenuator.

40. Calculate dynamic accuracy for each step by using the formula $|G - F|$. Place these values in the appropriate column of the "Performance Test Record."

In Case of Difficulty

1. If the analyzer fails the test at ALL power levels, be sure you followed the recommended attenuator settings as listed in the "Performance Test Record." Repeat this performance test.

2. If both test port measured values are out of specifications:

   a. Recalibrate the power meter.

   b. Repeat this performance test.

3. If the analyzer fails either test port 2 or test port 1 dynamic accuracy at lower power levels:

   a. Perform the "IF Amplifier Correction Constants" and "ADC Offset Correction Constants" procedures (located in Chapter 3, "Adjustments and Correction Constants").

   b. Repeat this performance test.

   c. If it still fails, replace the A10 Digital IF assembly.

   d. Repeat the two adjustment procedures mentioned in this step and then repeat this performance test.

14. Test Port Receiver Magnitude Compression

Specifications

Frequency Range	Test Port	Magnitude[1]
300 kHz to 3 GHz	Port 1	≤0.45 dB
3 GHz to 6 GHz[2]	Port 1	≤0.80 dB
300 kHz to 3 GHz	Port 2	≤0.45 dB
3 GHz to 6 GHz[2]	Port 2	≤0.80 dB

1 With a 10 Hz IF bandwidth.

2 Only for analyzers with Option 006 – 30 kHz to 6 GHz range.

Required Equipment for 50Ω Analyzers

Cable, APC-7, 24-inch HP P/N 8120-4779

Required Equipment for 75Ω Analyzers

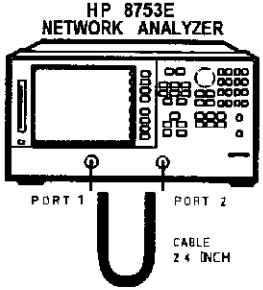
Cable, 75Ω, Type-N, 24-inch HP P/N 8120-2408

Analyzer warmup time: 1 **hour**

Perform this test to verify the compression/expansion magnitude levels of the analyzer's test port receiver samplers.

Test Port 2 Magnitude Compression

1. Connect the equipment as shown in Figure 2-40.



s/q6'8c

Figure 2-40. Test Port Magnitude Compression Test Setup

2. Press (Preset) (Meas) **Trans: FWD S21 (B/R)**.

3. Press (Avg) IF **BW** (10) (x1.

4. Press (Menu) **CW FREQ** (50) (M/μ).

5. Press SWEEP TYPE MENU POWER SWEEP START (-10) (x1.

6. Press (Menu] TRIGGER MENU SINGLE.

7. At the end of the sweep, press (Scale Ref) **AUTO** SCALE.

8. Press (Marker Fctn) **MKR** SEARCH SEARCH: MAX .

9. Press (Marker) MARKER 2 (Marker Fctn) **MKR** SEARCH **SEARCH:** MIN .

10. Press (Marker) **ΔMODE** MENU **ΔREF = 1** .

11. Write the absolute value of the marker 2 reading in the "Performance Test Record. "

12. Press (Menu) CW **FREQ** (1) (G/n).

13. Press TRIGGER MENU SINGLE.

14. At the end of the sweep, press (Scale Ref) **AUTO** SCALE.

15. Press (Marker) MARKER **ΔREF=1** (Marker Fctn) **MKR** SEARCH SEARCH: MAX .

16. Press (Marker) MARKER 2 (Marker) **MKR SEARCH** SEARCH: **MIN**.

17. Write the absolute value of marker 2 in the "Performance Test Record."

18. Repeat steps 12 through 17 for the other frequencies listed for Port 2 on the "Performance Test Record."

Test Port 1 Magnitude Compression

19. Press (Meas) **Trans: REV S12 (A/R)**.

20. Press (Menu) **CW FREQ** (50) (M/μ).

21. Press TRIGGER **MENU** SINGLE.

22. At the end of the sweep, press (Scale Ref) **AUTO** SCALE.

23. Press (Marker) MARKER **ΔREF =** 1 (Marker Fctn) **MKR SEARCH** SEARCH: MAX.

24. Press [Marker) MARKER 2 (Marker Fctn) **MKR SEARCH** SEARCH: **MIN**.

25. Write the absolute value of the marker 2 reading in the "Measured Value" column of the "Performance Test Record."

26. Repeat steps 20 through 25 for the other CW frequencies listed for Port 1 in the "Performance Test Record."

In Case of Difficulty

1. If the analyzer fails "Test Port 2 Magnitude Compression":
   a. Repeat this test.
   b. Replace the A6 B sampler assembly if the analyzer still fails the test.
2. If the analyzer fails "Test Port 1 Magnitude Compression":
   a. Repeat this test.
   b. Replace the A5 A sampler assembly if the analyzer still fails the test.

15. Test Port Receiver Phase Compression

Specifications

CW Frequency	Test Port	Phase[1]
300 kHz to 3 GHz	Port 1	≤6°
3 GHz to 6 GHz[2]	Port 1	≤7.5°
300 kHz to 3 GHz	Port 2	≤6°
3 GHz to 6 GHz[2]	Port 2	≤7.5°

1 With 10 Hz IF bandwidth.

2 Only for analyzer with Option 006 - 30 kHz to 6 GHz range.

Required Equipment for 503 Analyzers

Cable, **APC-7,** 24-inch HP P/N 8120-4779

Required Equipment for 753 Analyzers

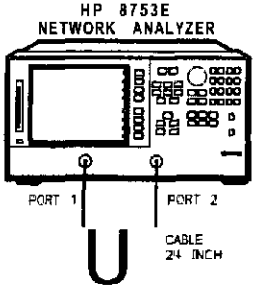
Cable, 75Ohm Type-N, 24-inch HP P/N 8120-2408

Analyzer warmup time: 1 **hour**

Perform this test to verify the compression/expansion phase relationships of the analyzer's test port receiver samplers.

Test Port 2 Phase Compression

1. Connect the equipment as shown in Figure 2-41.



g61Be

Figure 2-41. Test Port Phase Compression Test Setup

2. Press (Preset) (Meas) **Trans: FWD S21 (B/R)** (Format) **PHASE**.
3. Press (Avg) IF BW (10) (x1).
4. Press (Menu) SWEEP TYPE MENU **POWER** SWEEP START (-10) (x1).
5. Press [Menu) CW **FREQ** (50) (M/μ).
6. Press (Menu) TRIGGER **MENU SINGLE**.
7. At the end of the sweep, press (Scale Ref) AUTO SCALE.
8. Press (Marker Fctn) **MKR SEARCH SEARCH:** MAX.
9. Press (Marker') **MARKER 2** (Marker Fctn) **MKR SEARCH SEARCH: MIN**.
10. Press (Marker) **ΔMODE** MENU **ΔREF** = 1.
11. Write the absolute value of the marker 2 reading in the "Measured **Value**" column of the "Performance Test Record."
12. Repeat steps 5 to 11 for the other CW frequencies listed for Port 2 in the "Performance Test Record."

Test Port 1 Phase Compression

13. Press (Meas) **Trans:** REV **S12 (A/R)** [Format) PHASE.

14. Press (Menu) **CW FREQ** (50) (M/μ).

15. Press (Menu) TRIGGER **MENU SINGLE .**

16. At the end of the sweep, press (Scale Ref) **AUTO SCALE .**

17. Press (Marker) MARKER **AREF = 1** (Marker Fctn) **MKR SEARCH** SEARCH: MAX .

18. Press (Marker) **MARKER** 2 (Marker Fctn) **MKR** SEARCH **SEARCH: MIN .**

19. Write the absolute value of the marker 2 reading in the "Measured Value" column of the "Performance Test Record."

20. Repeat steps 14 to 19 for the other CW frequencies listed for Port 1 in the "Performance Test Record."

In Case of Difficulty

1. If the analyzer fails the "Test Port 2 Phase Compression" test:
   a. Repeat this test.
   b. Replace the A6 B sampler assembly if analyzer still fails the test.
2. If the analyzer fails the "Test Port 1 Phase Compression" test:
   a. Repeat this test.
   b. Replace the A5 A sampler assembly if analyzer still fails the test.

16. Test Port Output/Input Harmonics (Option 002 Analyzers without Option 006 Only)

Specifications

Test Port	Harmonic	Limit
Output	2nd	<−25 dBc @ + 10 dBm
Output	3rd	<−25 dBc @ +10 dBm
Input Port 1	2nd	<−15 dBc @ +8 dBm
Input Port 1	3rd	<−30 dBc @ +8 dBm
Input Port 2	2nd	<−15 dBc @ +8 dBm
Input Port 2	3rd	<−30 dBc @ +8 dBm

Equipment Required for 50 Ohm Analyzers

Cable, APC-7, 24-inch	HP P/N 8120-4779
Attenuator (2), 20 dB, APC-7	HP 8492A Option 020

Equipment Required for 75 Ohm Analyzers

Minimum Loss Pad (2)	.HP 11852B
Cable, Type-N	HP P/N 8120-2408
Attenuator (2), 20 dB, Type-N	.HP 8491A Option 020

Analyzer ***warmup time:*** 30 **minutes**

Perform this test to determine the spectral purity of the HP 87533 input and output test ports.

Note The test port input 3rd harmonic specifications are better than the test port output 3rd harmonic specifications.

Test Port Output Worst Case 2nd Harmonic

1. Press (Preset) (Menu) **POWER** (10) (x1).
2. Press (Start) (16) (M/μ) (Stop) (1.5) (G/n) to set the frequency range.
3. Press (Avg) IF **BW** (10) (x1) to set the IF bandwidth to 10 Hz.
4. Connect the equipment as **shown** in Figure 2-42.

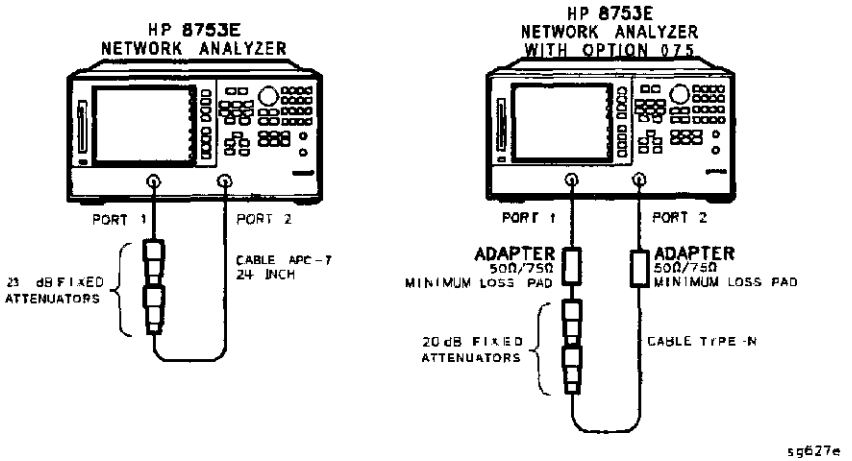


Figure 2-42. Test Port Output Harmonics Test Setup

5. Press (Meas) **Trans:REV S12 (A/R) INPUT** PORTS A.
6. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.
7. Press (System) **HARMONIC MEAS HARMONIC SECOND** .
8. After one sweep, press (Scale Ref) **AUTO** SCALE to get a better viewing of the trace.
9. Press (Marker Fctn) **MKR SEARCH** SEARCH MAX .

10. Write the marker 1 value (which appears on the analyzer display) on the "Performance Test Record." This is the worst case test port output 2nd harmonic.

Test Port Output Worst Case 3rd Harmonic

11. Press [Stop] [1] [G/n] to change the stop frequency to 1 GHz.
12. Press [System] **HARMONIC MEAS HARMONIC** OFF.
13. After one sweep, press [Display] **DATA→MEMORY DATA/MEM** to normalize the trace.
14. Press [Scale Ref] AUTO SCALE SCALE/NIV [1] [x1] to get a better viewing of the trace.
15. Press [System] **HARMONIC MEAS HARMONIC** THIRD.
16. After one sweep, press [Scale Ref] **AUTO** SCALE
17. Press [Marker Fctn] **MKR SEARCH SEARCH** MAX.
18. Write the marker 1 value on the "Performance Test Record."

Port 1 Input Worst Case 2nd Harmonic

19. Connect the equipment as shown in Figure 2-43.

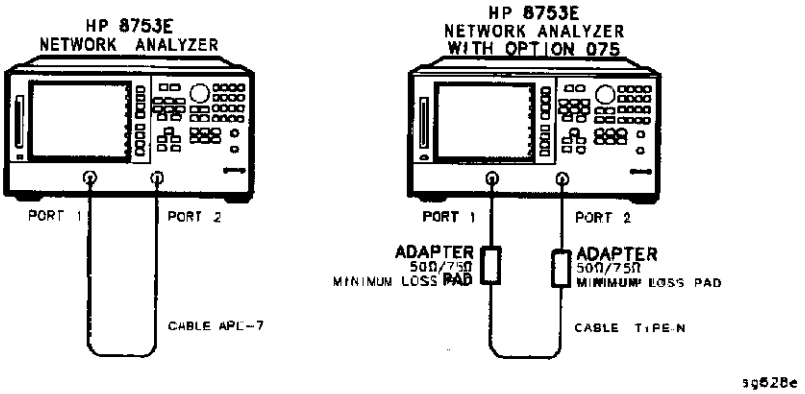


Figure 2-43. Receiver Harmonics Test Setup

20. Press (Preset) (Menu) **POWER** (8) (x1).

21. Press (Avg) IF **BW** (1) (0) (x1).

22. Press (Start) (16) (M/μ) (Stop) (1.5) (G/n) to set the frequency range.

23. Press (Meas) **Trans:REV S12 (A/R)** INPUT **PORTS** A.

24. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.

25. Press (System) HARMONIC **MEAS** HARMONIC SECOND.

26. After one sweep, press (Scale Ref) AUTO SCALE to get a better viewing of the trace.

27. Press (Marker Fctn) **MKR SEARCH SEARCH** MAX .

28. Write the marker 1 **value** (which appears on the analyzer display) on the "Performance Test Record." This is the worst case port 1 input (receiver channel A) 2nd harmonic.

Port 1 Input Worst Case 3rd Harmonic

29. Press (Stop) (1) (G/n) to change the stop frequency for measuring the receiver 3rd harmonic.

30. Press (System) HARMONIC **MEAS** HARMONIC OFF.

31. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.

32. Press (Scale Ref) AUTO SCALE SCALE/HIV (1) (x1) to get a better viewing of the trace.

33. Press (System) HARMONIC **MEAS** HARMONIC THIRD,

34. After one sweep, press (Scale Ref) **AUTO** SCALE.

35. Press (Marker Fctn) MKR SEARCH SEARCH MAX.

36. Write the marker 1 value on the "Performance Test Record."

37. Press (System) HARMONIC **MEAS** HARMONIC OFF.

Port 2 Input Worst Case 2nd Harmonic

38. Press (Stop) (1.5) (G/n) to set the stop frequency for measuring the 2nd harmonic.

39. Press (Meas) **Trans: FWD S21 (B/R)** INPUT **PORTS B**.

40. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.

41. Press (System) **HARMONIC MEAS** HARMONIC SECOND.

42. After one sweep, press (Scale Ref) **AUTO** SCALE to get a better viewing of the trace.

43. Press (Marker Fctn) **MKR** SEARCH SEARCH MAX.

44. Write the marker 1 value (which appears on the analyzer display) on the "Performance Test Record." This is the worst case port 2 input (receiver channel B) 2nd harmonic.

Port 2 Input Worst Case 3rd Harmonic

45. Press (Stop) (1) (G/n) to change the stop frequency for measuring the receiver 3rd harmonic.

46. Press (System) HARMONIC **MEAS** HARMONIC OFF .

47. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.

48. Press (Scale Ref) **AUTO SCALE SCALE/DIV** (1) (xl) to get a better viewing of the trace.

49. Press (System) **HARMONIC MEAS HARMONIC THIRD** .

50. After one sweep, press (Scale Ref) **AUTO** SCALE .

51. Press (Marker Fctn) **MKR SEARCH SEARCH** MAX .

52. Write the marker 1 value on the "Performance Test Record."

17. Test Port Output/Input Harmonics (Option 002 Analyzers with Option 006 Only)

Specifications

Test Port	Harmonic	Limit
Output	2nd	<–25 dBc @ +10 dBm
Output	3rd	<–25 dBc @ +10 dBm
Input Port 1	2nd	<–15 dBc @ +8 dBm
Input Port 1	3rd	<–30 dBc @ +8 dBm
Input Port 2	2nd	<–15 dBc @ +8 dBm
Input Port 2	3rd	<–30 dBc @ + 8 dBm

Equipment Required

Cable, APC-7, 24-inch ..... HP P/N 8120-4779
Attenuator (2), 20 dB ..... HP 8492A Opt 020

Analyzer warmup time: **30 minutes**

Perform this test to determine the spectral purity of the HP 87533 input and output test ports.

Note The test port input 3rd harmonic specifications are ***better*** than the test port output 3rd harmonic specifications.

Test Port Output Worst Case 2nd Harmonic

1. Press (Preset) (Menu) **POWER** (10) (x1) to set the test port power to + 10 dBm.
2. Press (Start) (16) (M/μ) (Stop) (3) (G/n) to set the frequency range.
3. Press (Avg) IF BW (10) (x1) to set the IF bandwidth to 10 Hz.
4. Connect the equipment as shown in Figure 2-44.

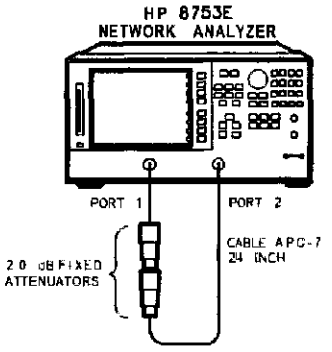


Figure Z-44 **Test** Port Output Harmonics **Test** Setup

5. Press (Meas) **Trans:REV S12(A/R)** INPUT **PORTS** A.
6. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.
7. Press (System) HARMONIC **MEAS HARMONIC SECOND**.
8. After one sweep, press (Scale Ref) **AUTO** SCALE to get a better viewing of the trace.
9. Press (Marker) MKH **SEARCH SEARCH** MAX.
10. Write the marker 1 value (which appears on the **analyzer** display) on the "Performance Test Record." This is the worst case test port output 2nd harmonic.

Test Port Output Worst Case 3rd Harmonic

11. Press (Stop) (2) (G/n) to change the stop frequency to 2 GHz.
12. Press (System) HARMONIC **MEAS** HARMONIC OFF .
13. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.
14. Press (Scale Ref) AUTO SCALE **SCALE/DIV** (1) (xl) to get a better viewing of the trace.
15. Press (System) **HARMONIC MEAS** HARMONIC THIRD.
16. After one sweep, press (Scale Ref) **AUTO** SCALE.
17. Press (Marker Fctn) MKR **SEARCH** SEARCH MAX .
18. Write the marker 1 value on the "Performance Test Record."

Port 1 Input Worst Case 2nd Harmonic

19. Connect the equipment as shown in Figure 2-45.

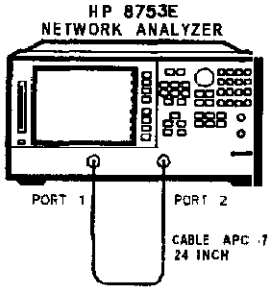


Figure 2-45. Receiver Harmonics Test Setup

20. Press (Preset) (Menu) **POWER** (8) (x1).
21. Press (Avg) IF **BW** (10) (x1).
22. Press (Start) (16) (M/μ) (Stop) (3) (G/n) to set the frequency range.
23. Press (Meas) **Trans :REV S12 (A/R) INPUT PORTS** A.
24. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.
25. Press (System) HARMONIC **MEAS HARMONIC SECOND**.
26. After one sweep, press (Scale Ref) **AUTO** SCALE to get a better viewing of the trace.
27. Press (Marker Fctn) **MKR SEARCH** SEARCH: **MAX**.
28. Write the marker 1 value (which appears on the analyzer display) on the "Performance Test Record." This is the worst case port 1 input (receiver channel A) 2nd harmonic.

Port 1 Input Worst Case 3rd Harmonic

29. Press (Stop) (2) (G/n) to change the stop frequency for measuring the receiver 3rd harmonic.
30. Press (System) HAHMONIC **MEAS** HAHMONIC OFF .
31. After one sweep, press (Display) **DATA→MEMORY** DATAIMEM to normalize the trace.
32. Press (Scale Ref) AUTO SCALE **SCALE/DIV** (1) (x1) to get a better viewing of the trace.
33. Press (System) HAHMONIC **MEAS** HAHMONIC THIRD.
34. After one sweep, press (Scale Ref) AUTO SCALE
35. Press (Marker Fctn) MKR SEAHCH SEAHCH: MAX .
36. Write the marker 1 value on the "Performance 'lest Record. "
37. Press (System) HAHMONIC **MEAS** HAHMONIC OFF.

Port 2 Input Worst Case 2nd Harmonic

38. Press (Stop) (3) (G/n) to set the stop frequency for measuring the 2nd harmonic.
39. Press (Meas) **Trans:FWD S21 (B/R)** INPUT PORTS B .
40. After one sweep, press (Display) DATA-MEMORY **DATA/MEM** to normalize the trace.
41. Press (System) HAHMONIC **MEAS HARMONIC** SECOND.
42. After one sweep, press (Scale Ref) AUTO SCALE to get a better viewing of the trace.
43. Press (Marker Fctn) MKR SEAHCH SEAHCH MAX.
44. Write the marker 1 value (which appears on the analyzer display) on the "Performance 'lest Record." This is the worst case port 2 input (receiver channel B) 2nd harmonic.

Port 2 Input Worst Case 3rd Harmonic

45. Press (Stop) (2) (G/n) to change the stop frequency for measuring the receiver 3rd harmonic.

46. Press (System) HARMONIC **MEAS** HARMONIC OFF.

47. After one sweep, press (Display) **DATA→MEMORY DATA/MEM** to normalize the trace.

48. Press (Scale Ref) AUTO SCALE **SCALE/DIV** (1) (x1) to get a better viewing of the trace.

49. Press (System) HARMONIC **MEAS HARMONIC** THIRD.

50. After one sweep, press (Scale Ref) AUTO SCALE.

51. Press (Marker Fctn) **MKR SEARCH** SEARCH: MAX .

52. Write the marker 1 value on the "Performance Test Record. "

2a

Performance Test Record

For Analyzers with a Frequency Range of
30 **kHz** to 3 **GHz**

Note See the next "Performance Test Record" section if your analyzer frequency range is from 30 kHz to 6 GHz (Option 006).

HP 87533 Performance Test Record (1 of 12)

Calibration Lab Address:

Report Number _____

Date _____

_____ Last Calibration Date _____

_____ Customer's Name _____

_____ Performed by _____

Model HP 87533

Serial No. _____ Option(s) _____

Firmware Revision _____

Ambient Temperature _____° C Relative Humidity _____%

Test Equipment Used:

Description	**Model Number**	**Trace Number Cal Due Date**
Frequency Counter	_____	_____
Power Meter	_____	_____
Power Sensor	_____	_____
Calibration Kit	_____	_____
Verification Kit	_____	_____

Notes/Comments: _____

_____

_____

HP 87533 Performance Test Record (2 of 12)
For 30 **kHz—3 GHz** Analyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	Report Number _____ **Date** _____

▶▶ 1. Test Port Output Frequency Range and Accuracy

CW Frequencies (MHz)	Min. (MHz)	Results Measured (MHz)	Max. (MHz)	Measurement Uncertainty (MHz)
0.03	0.029 999 7	_____	0.030 000 3	± 0.000 000 050
0.3	0.299 997	_____	0.300 003	± 0.000 000 520
5.0	4.999 950	_____	5.000 050	± 0.000 009
16.0	15.999 840	_____	16.000 160	± 0.000 028
31.0	30.999 690	_____	31.000 310	± 0.000 054
60 999 999	60.999 390	_____	61.000 610	± 0.000 105
121.0	120.998 790	_____	121.001 210	± 0.000 207
180.0	179.998 200	_____	180.001 800	± 0.000 307
310.0	309.995 900	_____	310.003 100	± 0.000 528
700.0	699.930 000	_____	700.007 000	± 0.001 192
1 300.0	1 299.987	_____	1 300.013	± 0.002 212
2 000.0	1 999.980	_____	2 000.020	± 0.003 403
3 000.0	2 999.970	_____	3 000.030	± 0.005 104

▶▶ 2. External Source Mode Frequency Range

Test Frequencies (GHz)	Results
0.010	_____
0.020	_____
0.100	_____
1.000	_____
2.000	_____
3.000	_____

HP 87533 Performance Test Record (3 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company Model HP 8753E Serial Number _____	Report Number _____ Date _____

▶▶3. Test Port Output Power Accuracy

Test Frequencies	Test Port output Power (dBm)	Specification (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
Center Frequency				
300 kHz	0	± 1	_____	± 0.465
20 MHz	0	± 1	_____	± 0.10
50 MHz	0	± 1	_____	± 0.10
100 MHz	0	± 1	_____	± 0.10
200 MHz	0	± 1	_____	± 0.10
500 MHz	0	± 1	_____	± 0.10
1 GHz	0	± 1	_____	± 0.13
2 GHz	0	± 1	_____	± 0.13
3 GHz	0	± 1	_____	± 0.27

▶▶4. Test Port Output Power Range and Linearity

Test Settings	Results Measured (dB)	Power Level Linearity (dB)	Specification (dB)	Measurement Uncertainty (dB)
CW Frequency = 300 kHz				
− 15	_____	_____	± 0.2	± 0.03
− 13	_____	_____	± 0.2	± 0.03
− 11	_____	_____	± 0.2	± 0.03
- 9	_____	_____	± 0.2	± 0.02
- 7	_____	_____	± 0.2	± 0.02
- 5	_____	_____	± 0.2	± 0.02
- 3	_____	_____	± 0.2	± 0.02
- 1	_____	_____	± 0.2	± 0.02
+ 1	_____	_____	± 0.2	± 0.03
+ 3	_____	_____	± 0.2	± 0.03
+ 5	_____	_____	± 0.5	± 0.03

HP 87533 Performance Test Record (4 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	**Report Number,** _____ **Date** _____

▶▶ 4. Test Port Output Power Range and Linearity (continued)

Test Settings	Results Measured (dB)	Power Level Linearity (dB)	Specification (dB)	Measurement Uncertainty (dB)
+ 7	_____	_____	± 0.5	± 0.03
+ 9	_____	_____	± 0.5	± 0.03
+ 10	_____	_____	± 0.5	± 0.03
CW Frequency = 3 GHz				
− 15	_____	_____	± 0.2	± 0.03
− 13	_____	_____	± 0.2	± 0.03
− 11	_____	_____	± 0.2	± 0.03
− 9	_____	_____	± 0.2	± 0.02
− 7	_____	_____	± 0.2	± 0.02
− 5	_____	_____	± 0.2	± 0.02
− 3	_____	_____	± 0.2	± 0.02
− 1	_____	_____	± 0.2	± 0.02
+ 1	_____	_____	± 0.2	± 0.03
+ 3	_____	_____	± 0.2	± 0.03
+ 5	_____	_____	± 0.5	± 0.03
+ 7	_____	_____	± 0.5	± 0.03
+ 9	_____	_____	± 0.5	± 0.03
+ 10	_____	_____	± 0.5	± 0.03

HP 87533 Performance Test Record (5 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 5. Minimum R Channel Level

CW Frequency	Specification (dB)	Test Port Power	Measurement Uncertainty (dB)
300 kHz	< −35	_____	± 1.0
3.29 MHz	< −35	_____	± 1.0
3.31 MHz	< −35	_____	± 1.0
15.90 MHz	< −35	_____	± 1.0
16.10 MHz	< −35	_____	± 1.0
30.90 MHz	< −35	_____	± 1.0
31.10 MHz	< −35	_____	± 1.0
1.6069 GHz	< −35	_____	± 1.0
1.6071 GHz	< −35	_____	± 1.0
3.000 GHz	< −35	_____	± 1.0

▶▶ 6. Test Port Input Noise Floor Level

Frequency Range	Test Port	IF Bandwidth	Specification (dBm)	Calculated Value	Measurement Uncertainty
300 kHz - 3 GHz	Port 1	3 kHz	− 82	_____	N/A
300 kHz - 3 GHz	Port 1	10 Hz	− 102	_____	N/A
300 kHz - 3 GHz	Port 2	10 Hz	− 102	_____	N/A
300 kHz - 3 GHz	Port 2	3 kHz	− 82	_____	N/A

HP 87533 Performance **Test** Record (6 of 12)
For 30 **kHz—3 GHz** Analyzers

Hewlett-Packard Company	**Report Number** _____
Model HP 8753E	
Serial Number _____	**Date** _____

▶▶ 7. Test Port Input Frequency Response

Frequency Range	**Test Port**	**Specification (dB)**	**Measured Value (dB)**	**Measurement Uncertainty (dB)**
300 kHz—3 GHz	Port 2	± 1	_____	0.47
300 kHz—3 GHz	Port 1	± 1	_____	0.47

▶▶ 8. Test Port Crosstalk

Test Settings	**Specification (dB)**	**Measured Value (dB)**	**Measurement Uncertainty**
Crosstalk to Test Port 2			
300 kHz—3 GHz	< −100	_____	N/A
Crosstalk to Test Port 1			
300 kHz—3 GHz	< −100	_____	N/A

HP 87533 Performance Test Record (7 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company **Model HP 87533** **Serial Number** _____	**Report Number** _____ **Date** _____

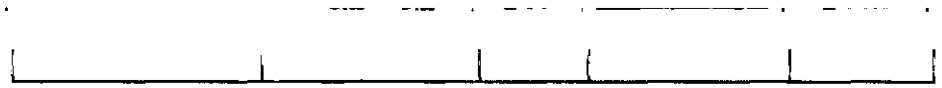
▶▶ 9. Calibration Coefficients

Test Description	Frequency Range	Spec. (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
Forward Direction				
Directivity	300 kHz - 1.3 GHz	≥ 35	_____	± 0.9
Directivity	1.3 GHz - 3 GHz	≥ 30	_____	± 0.8
Forward Direction				
Source Match	300 kHz - 1.3 GHz	≥ 16	_____	± 0.2
Source Match	1.3 GHz - 3 GHz	≥ 16	_____	± 0.2
Forward Direction				
Trans Tracking	300 kHz - 1.3 GHz	± 1.5	_____	± 0.006
Trans Tracking	1.3 GHz - 3 GHz	± 1.5	_____	± 0.009
Forward Direction				
Refl. Tracking	300 kHz - 1.3 GHz	± 1.5	_____	± 0.001
Refl. Tracking	1.3 GHz - 3 GHz	± 1.5	_____	± 0.005
Reverse Direction				
Load Match	300 kHz - 1.3 GHz	≥ 18	_____	± 0.1
Load Match	1.3 GHz - 3 GHz	≥ 16	_____	± 0.2

Hewlett-Packard Company	Report Number _____
Model HP 8753E	
Serial Number _____	**Date** _____

▶▶ 9. Calibration Coefficients (continued)

Test Description	**Frequency Range**	**Spec. (dB)**	**Measured Value (dB)**	**Measurement Uncertainty (dB)**
Reverse Direction				
Trans. Tracking	300 kHz - 1.3 GHz	± 1.5	_____	± 0.006
Trans. Tracking	1.3 GHz - 3 GHz	± 1.5	_____	± 0.009
Forward Direction				
Load Match	300 kHz - 1.3 GHz	≥ 18	_____	± 0.1
Load Match	1.3 GHz - 3 GHz	≥ 16	_____	± 0.2
Reverse Direction				
Directivity	300 kHz - 1.3 GHz	≥ 35	_____	± 0.9
Directivity	1.3 GHz - 3 GHz	≥ 30	_____	± 0.8
Reverse Direction				
Source Match	300 kHz - 1.3 GHz	≥ 16	_____	± 0.2
Source Match	1.3 GHz - 3 GHz	≥ 16	_____	± 0.2
Reverse Direction				
Refl Tracking	300 kHz - 1.3 GHz	± 1.5	_____	± 0.001
Refl Tracking	1.3 GHz - 3 GHz	± 1.5	_____	± 0.005



HP 87533 Performance Test Record (9 of 12)
For 30 kHz—3 GHz 4nalyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 10. System Trace Noise

CW Frequency (GHz)	Ratio	Specification	Measured Value	Measurement Uncertainty
3	A/R	< 0.006 dBrms	_____	±0.001 dB
3	A/R	< 0.038° rms	_____	±0.01°
3	B/R	< 0.006 dB rms	_____	±0.001 dB
3	B/R	< 0.038° rms	_____	±0.01°

▶▶ 12. Test Port Input Impedance

Frequency Range	Test Port	Return Loss (dB)	Specification (dB)	Measurement Uncertainty (dB)
300 kHz—1.3 GHz	Port 2	_____	≥ 18	± 1.5
1.3 GHz—3 GHz	Port 2	_____	≥ 16	± 1.5
300 kHz—1.3 GHz	Port 1	_____	≥ 18	± 1.5
1.3 GHz—3 GHz	Port 1	_____	≥ 16	± 1.5

HP 87533 Performance Test Record (10 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company **Model HP 87533** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 13. Test Port Receiver Magnitude Dynamic Accuracy

		G	F	|G – F|		
Test Port Input Power	**8496A Attn. (dB)**	**Test Port Measurement (dBm)**	**Expected Measurement (corrected) (dBm)**	**Dynamic Accuracy (Calculated)**	**Spec. (dB)**	**Meas. Uncer. (dB)**
Test Port 2						
– 10	0	_____	_____	_____	≤ 0.033	± 0.008
– 20 (Ref)	10	Reference	Reference	Reference	Reference	Reference
– 30	20	_____	_____	_____	≤ 0.031	± 0.008
– 40	30	_____	_____	_____	≤ 0.042	± 0.008
– 50	40	_____	_____	_____	≤ 0.057	± 0.008
– 60	50	_____	_____	_____	≤ 0.098	± 0.017
– 70	60	_____	_____	_____	≤ 0.247	± 0.017
– 80	70	_____	_____	_____	≤ 0.725	± 0.017
– 90	80	_____	_____	_____	≤ 2.097	± 0.017
– 100	90	_____	_____	_____	≤ 5.399	± 0.027
Test Port 1						
– 10	0	_____	_____	_____	≤ 0.033	± 0.008
– 20 (Ref)	10	Reference	Reference	Reference	Reference	Reference
– 30	20	_____	_____	_____	≤ 0.031	± 0.008
– 40	30	_____	_____	_____	≤ 0.042	± 0.008
– 50	40	_____	_____	_____	≤ 0.057	± 0.008
– 60	50	_____	_____	_____	≤ 0.098	± 0.017
– 70	60	_____	_____	_____	≤ 0.247	± 0.017
– 80	70	_____	_____	_____	≤ 0.725	± 0.017
– 90	80	_____	_____	_____	≤ 2.097	± 0.017
– 100	90	_____	_____	_____	≤ 5.399	± 0.027

HP 87533 Performance Test Record (11 of 12)
For 30 kHz—3 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 14. Test Port Receiver Magnitude Compression

CW Frequency	Test Port	Measured Value (dB)	Specification (dB)	Measurement Uncertainty
50 MHz	Port 2	_____	≤ 0.45	N/A
1 GHz	Port 2	_____	≤ 0.45	N/A
2 GHz	Port 2	_____	≤ 0.45	N/A
3 GHz	Port 2	_____	≤ 0.45	N/A
50 MHz	Port 1	_____	≤ 0.45	N/A
1 GHz	Port 1	_____	≤ 0.45	N/A
2 GHz	Port 1	_____	≤ 0.45	N/A
3 GHz	Port 1	_____	≤ 0.45	N/A

▶▶ 15. Test Port Receiver Phase Compression

CW Frequency	Test Port	Measured Value (degrees)	Specification (degrees)	Measurement Uncertainty
50 MHz				

50 MHz	Port 2	———————	≤ 6°	N/A
1 GHz	Port 2	———————	≤ 6°	N/A
2 GHz	Port 2	———————	≤ 6°	N/A
3 GHz	Port 2	———————	≤ 6°	N/A
	Port 1	———————	≤ 6°	N/A
1 GHz	Port 1	———————	≤ 6°	N/A
2 GHz	Port 1	———————	≤ 6°	N/A
3 GHz	Port 1	———————	≤ 6°	N/A

HP 87533 Performance **Test** Record (12 of 12)
For 30 **kHz—3 GHz** Analyzers

Hewlett-Packard Company **Model HP 8753E** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 16. Test Port Output/Input Harmonics (Option 002 without Option 006)

Test Description	Specification (dBc)	Measurement Value (dBc)	Measurement Uncertainty (dB)
Test Port output Harmonics			
2nd	≤ 25	_____	± 1.5
3rd	≤ 25	_____	± 1.5
Port 1 Input Harmonics			
2nd	≤ 15	_____	± 1.5
3rd	≤ 30	_____	± 1.5
Port 2 Input Harmonics			
2nd	≤ 15	_____	± 1.5
3rd	≤ 30	_____	± 1.5

2b

Performance Test Record

For Analyzers with a Frequency Range of 30 kHz to 6 GHz

Note	See the previous "Performance Test Record" section if your analyzer frequency range is from 30 kHz to 3 GHz.

HP 87533 Performance Test Record (1 of 14)

Calibration Lab Address:

Report Number _____

Date _____

_____ Last Calibration Date _____

_____ Customer's Name _____

_____ Performed by _____

Model HP 87533 Option 006

Serial No. _____ Option(s) _____

Firmware Revision _____

Ambient Temperature _____ ° C Relative Humidity _____ %

Test Equipment Used:

Description	Model Number	Trace Number	Cal Due Date
Frequency Counter			
Power Meter			
Power Sensor			
Calibration Kit			
Verification Kit			

Notes/Comments: _____

HP 87533 Performance **Test** Record (2 of 14)
For 30 **kHz—6 GHz** Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial** Number _____	**Report Number** _____ **Date** _____

▶▶ 1. Test Port Output Frequency Range and Accuracy

Test Frequencies (MHz)	Min. (MHz)	Results Measured (MHz)	Max. (MHz)	Measurement Uncertainty (MHz)
0.03	0.029 999 7	_____	0.030 000 3	± 0.000 000 050
0.3	0.299 997	_____	0.300 003	± 0.000 000 520
5.0	4.999 950	_____	5.000 050	± 0.000 009
16.0	15.999 840	_____	16.000 160	± 0.000 028
31.0	30.999 690	_____	31.000 310	± 0.000 054
60.999 999	60.999 390	_____	61.000 610	± 0.000 105
121.0	120.998 790	_____	121.001 210	± 0.000207
180.0	179.998 200	_____	180.001 800	± 0.000 307
310.0	309.996 900	_____	310.003 100	± 0.000 528
700.0	699.930 000	_____	700.007 000	± 0.001 192
1 300.0	1 299.987	_____	1 300.013	± 0.002 212
2 000.0	1 999.980	_____	2 000.020	± 0.003 403
3 000.0	2 999.970	_____	3 000.030	± 0.005 104
4.0	3.999 960	_____	4.000 040	± 0.006 805
5.0	4.999 950	_____	5.000 050	± 0.008 506
6.0	5.999 940	_____	6.000 060	± 0.010 207

HP 87533 Performance Test Record (3 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial** Number _____	**Report Number** _____ **Date** _____

▶▶ 2. External Source Mode Frequency Range

Test Frequencies (GHz)	Result
0.010	_____
0.020	_____
0.100	_____
1.000	_____
2.000	_____
3.000	_____
4.000	_____
5.000	_____
6.000	_____

▶▶ 3. Test Port Output Power Accuracy

Test Frequency	Test Port Output Power (dBm)	Specification (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
300 kHz	0	± 1	_____	± 0.47
20 MHz	0	± 1	_____	± 0.25
50 MHz	0	± 1	_____	± 0.12
100 MHz	0	± 1	_____	± 0.12
200 MHz	0	± 1	_____	± 0.12
500 MHz	0	± 1	_____	± 0.12
1 GHz	0	± 1	_____	± 0.12
2 GHz	0	± 1	_____	± 0.15
3 GHz	0	± 1	_____	+ 0.15
			_____	
			_____	
			_____	

4 GHz	0	± 1		± 0.17
5 GHz	0	± 1		± 0.17
6 GHz	0	± 1		± 0.17

HP 87533 Performance Test Record (4 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006**	**Report Number** _____
Serial Number _____	**Date** _____

▶▶ 4. Test Port Output Power Range and Linearity

Test Settings	Results Measured (dB)	Power Level Linearity (dB)	Specification (dB)	Meas. Uncert. (dB)
CW Frequency = 300 kHz				
− 15	_____	_____	± 0.2	± 0.03
− 13	_____	_____	± 0.2	± 0.03
− 11	_____	_____	± 0.2	± 0.03
- 9	_____	_____	± 0.2	± 0.02
- 7	_____	_____	± 0.2	± 0.02
- 5	_____	_____	± 0.2	± 0.02
- 3	_____	_____	± 0.2	± 0.02
- 1	_____	_____	± 0.2	± 0.02
+ 1	_____	_____	± 0.2	± 0.03
+ 3	_____	_____	± 0.2	± 0.03
+ 5	_____	_____	± 0.5	± 0.03
+ 7	_____	_____	± 0.5	± 0.03
+ 9	_____	_____	± 0.5	± 0.03
+ 10	_____	_____	± 0.5	± 0.03
CW Frequency = 3 GHz				
− 15	_____	_____	± 0.2	± 0.03
− 13	_____	_____	± 0.2	± 0.03
− 11	_____	_____	± 0.2	± 0.03
- 9	_____	_____	± 0.2	± 0.02
- 7	_____	_____	± 0.2	± 0.02
- 5	_____	_____	± 0.2	± 0.02
- 3	_____	_____	± 0.2	± 0.02
- 1	_____	_____	± 0.2	± 0.02
+ 1	_____	_____	± 0.2	± 0.03
+ 3	_____	_____	± 0.2	± 0.03
+ 5	_____	_____	± 0.5	± 0.03

HP 87533 Performance Test Record (5 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company Model HP 8753E Option 006 Serial Number _____	Report Number _____ Date _____

▶▶ 4. Test Port Output Power Range and Linearity (continued)

Test Settings	Results Measured (dB)	Power Level Linearity (dB)	Specification (dB)	Meas. Uncert. (dB)
+ 7	_____	_____	± 0.5	± 0.03
+ 9	_____	_____	± 0.5	± 0.03
+ 10	_____	_____	± 0.5	± 0.03
CW Frequency = 6 GHz				
− 15	_____	_____	± 0.2	± 0.03
− 13	_____	_____	± 0.2	± 0.03
− 11	_____	_____	± 0.2	± 0.03
− 9	_____	_____	± 0.2	± 0.03
− 7	_____	_____	± 0.2	± 0.02
− 5	_____	_____	± 0.2	± 0.02
− 3	_____	_____	± 0.2	± 0.02
− 1	_____	_____	± 0.2	± 0.02
+ 1	_____	_____	± 0.2	± 0.02
+ 3	_____	_____	± 0.2	± 0.03
+ 5	_____	_____	± 0.5	± 0.03
+ 7	_____	_____	± 0.5	± 0.03
+ 9	_____	_____	± 0.5	± 0.03
+ 10	_____	_____	± 0.5	± 0.03

HP 87533 Performance Test Record (6 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006**	Report Number _____
Serial Number _____	**Date** _____

▸▸ 5. Minimum R Channel Level

CW Frequency	Specification (dB)	Test Port Power	Measurement Uncertainty (dB)
300 kHz	< −35	_____	± 1.0
3.29 MHz	< −35	_____	± 1.0
3.31 MHz	< −35	_____	± 1.0
15.90 MHz	< −35	_____	± 1.0
16.10 MHz	< −35	_____	± 1.0
30.90 MHz	< −35	_____	± 1.0
31.10 MHz	< −35	_____	± 1.0
1.6069 GHz	< −35	_____	± 1.0
1.6071 GHz	< −35	_____	± 1.0
3.000 GHz	< −35	_____	± 2.0
4.000 GHz	< −30	_____	± 2.0
5.000 GHz	< −30	_____	± 2.0
6.000 GHz	< −30	_____	± 2.0

▸▸ 6. Test Port Input Noise Floor Level

Frequency Range	Test Port	IF Bandwidth	Specification (dBm)	Calculated Value	Measurement Uncertainty
300				_____	
300				_____	
300				_____	
300				_____	
3 GHz-6				_____	
3 GHz-6				_____	
3 GHz-6				_____	
3 GHz-6				_____	

kHz—3 GHz	Port 1	3 kHz	– 82	_____	N/A
kHz—3 GHz	Port 1	10 Hz	– 102	_____	N/A
kHz—3 GHz	Port 2	10 Hz	– 102	_____	N/A
kHz—3 GHz	Port 2	3 kHz	– 82	_____	N/A
GHz	Port 2	3 kHz	– 77	_____	N/A
GHz	Port 2	10 Hz	– 97	_____	N/A
GHz	Port 1	10 Hz	– 97	_____	N/A
GHz	Port 1	3 kHz	– 77	_____	N/A

HP 87533 Performance Test Record (7 of 14)
For 30 kHz—6 GHz 4nalyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 7. Test Port Input Frequency Response

Frequency Range	Test Port	Specification (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
300 kHz—3 GHz	Port 2	± 1	_____	0.47
300 kHz—3 GHz	Port 1	± 1	_____	0.47
3 GHz-6 GHz	Port 1	± 2	_____	0.17
3 GHz-6 GHz	Port 2	± 2	_____	0.17

▶▶ 8. Test Port Crosstalk

Test Settings	Specification (dB)	Measured Value (dB)	Measurement Uncertainty
Crosstalk to Test Port 2 300 kHz—3 GHz	< −100	_____	N/A
Crosstalk to Test Port 1 300 kHz—3 GHz	< −100	_____	N/A
Crosstalk to Test Port 1 3 GHz-6 GHz	< −90	_____	N/A
Crosstalk to Test Port 2 3 GHz—6 GHz	< −90	_____	N/A

HP 87533 Performance Test Record (8 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006**	**Report Number** _____
Serial Number _____	**Date** _____

▶▶ 9. Calibration Coefficients

Test Description	Frequenc y Range	Spec. (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
Forward Direction				
Directivity	300 kHz— 1 3 GHz	≥ 35	_____	± 0.9
Directivity	1.3 GHz-3 GHz	≥ 30	_____	± 0.8
Directivity	3 GHz--6 GHz	≥ 25	_____	± 0.8
Forward Direction				
Source Match	300 kHz—1 3 GHz	≥ 16	_____	± 0.2
Source Match	1.3 GHz—3 GHz	≥ 16	_____	± 0.2
Source Match	3 GHz--6 GHz	≥ 14	_____	± 0.3
Forward Direction				
Trans. Tracking	300 kHz—1.3 GHz	± 1.5	_____	± 0.006
Trans. Tracking	1.3 GHz-3 GHz	± 1.5	_____	± 0.009
Trans. Tracking	3 GHz-6 GHz	± 2.5	_____	± 0.021
Forward Direction				
Refl. Tracking	300 kHz— 1 3 GHz	± 1.5	_____	± 0.001
Refl. Tracking	1 3 GHz-3 GHz	± 1.5	_____	± 0.005
Refl. Tracking	3 GHz-6 GHz	± 2.5	_____	± 0.020
Reverse Direction				
Load Match	300 kHz— 1 3 GHz	≥ 18	_____	± 0 1
Load Match	1 3 GHz-3 GHz	≥ 16	_____	± 0 2
Load Match	3	14	_____	0 2

HP 87533 Performance Test Record (9 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006**	**Report Number** _____
Serial Number _____	**Date** _____

▶▶ 9. Calibration Coefficients (continued)

Test Description	Frequency Range	Spec. (dB)	Measured Value (dB)	Measurement Uncertainty (dB)
Reverse Direction				
Trans. Tracking	300 kHz– 1.3 GHz	± 1.5	_____	± 0.006
Trans. Tracking	1.3 GHz—3 GHz	± 1.5	_____	± 0.009
Trans. Tracking	3 GHz-6 GHz	± 2.5	_____	± 0.021
Forward Direction				
Load Match	300 kHz—1.3 GHz	≥ 18	_____	± 0.1
Load Match	1.3 GHz—3 GHz	≥ 16	_____	± 0.2
Load Match	3 GHz-6 GHz	≥ 14	_____	± 0.2
Reverse Direction				
Directivity	300 kHz– 1.3 GHz	≥ 35	_____	± 0.9
Directivity	1.3 GHz—3 GHz	≥ 30	_____	± 0.8
Directivity	3 GHz—6 GHz	≥ 25	_____	± 0.8
Reverse Direction				
Source Match	300 kHz - 1.3 GHz	≥ 16	_____	± 0.2
Source Match	1.3 GHz - 3 GHz	≥ 16	_____	± 0.2
Source Match	3 GHz - 6 GHz	≥ 14	_____	± 0.3
Reverse Direction				
Refl. Tracking	300 kHz - 1.3 GHz	± 1.5	_____	± 0.001
Refl. Tracking	1.3 GHz - 3 GHz	± 1.5	_____	± 0.005
Refl. Tracking	3 GHz - 6 GHz	± 2.5	_____	± 0.020

HP 87533 Performance Test Record (11 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial Number** _____	**Report Number** _____ **Date** _____

13. Test Port Receiver Magnitude Dynamic Accuracy

		G	F	|G − F|		
Test Port Input Power	**8496A Attn. (dB)**	**Test Port Measurement (dBm)**	**Expected Measurement (corrected) (dBm)**	**Dynamic Accuracy (Calculated)**	**Spec. (dB)**	**Meas. Uncer. (dB)**
Test Port 2						
− 10	0	_____	_____	_____	≤ 0.033	± 0.008
− 20 (Ref)	10	Reference	Reference	Reference	Reference	Reference
− 30	20	_____	_____	_____	≤ 0.031	± 0.008
− 40	30	_____	_____	_____	≤ 0.042	± 0.008
− 50	40	_____	_____	_____	≤ 0.057	± 0.008
− 60	50	_____	_____	_____	≤ 0.098	± 0.017
− 70	60	_____	_____	_____	≤ 0.247	± 0.017
− 80	70	_____	_____	_____	≤ 0.725	± 0.017
− 90	80	_____	_____	_____	≤ 2.097	± 0.017
− 100	90	_____	_____	_____	≤ 5.399	± 0.027
Test Port 1						
− 10	0	_____	_____	_____	≤ 0.033	± 0.008
− 20 (Ref)	10	Reference	Reference	Reference	Reference	Reference
− 30	20	_____	_____	_____	≤ 0.031	± 0.008
− 40	30	_____	_____	_____	≤ 0.042	± 0.008
− 50	40	_____	_____	_____	≤ 0.057	± 0.008
− 60	50	_____	_____	_____	≤ 0.098	± 0.017
− 70	60	_____	_____	_____	≤ 0.247	± 0.017
− 80	70	_____	_____	_____	≤ 0.725	± 0.017
− 90	80	_____	_____	_____	≤ 2.097	± 0.017
[illegible]	[illegible]	_____	_____		[illegible]	[illegible]

HP 8 7533 Performance **Test** Record (12 of 14)
For 30 **kHz—6 GHz** Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 14. Test Port Receiver Magnitude Compression

CW Frequency	Test Port	Measured Value (dB)	Specification (dB)	Measurement Uncertainty
50 MHz	Port 2	_____	≤ 0.45	N/A
1 GHz	Port 2	_____	≤ 0.45	N/A
2 GHz	Port 2	_____	≤ 0.45	N/A
3 GHz	Port 2	_____	≤ 0.45	N/A
4 GHz	Port 2	_____	≤ 0.80	N/A
5 GHz	Port 2	_____	≤ 0.80	N/A
6 GHz	Port 2	_____	≤ 0.80	N/A
50 MHz	Port 1	_____	≤ 0.45	N/A
1 GHz	Port 1	_____	≤ 0.45	N/A
2 GHz	Port 1	_____	≤ 0.45	N/A
3 GHz	Port 1	_____	≤ 0.45	N/A
4 GHz	Port 1	_____	≤ 0.80	N/A
5 GHz	Port 1	_____	≤ 0.80	N/A
6 GHz	Port 1	_____	≤ 0.80	N/A

HP 87533 Performance **Test** Record (13 of 14)
For 30 **kHz—6 GHz** Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 15. Test Port Receiver Phase Compression

CW Frequency	Test Port	Measured Value (degrees)	Specification (degrees)	Measurement Uncertainty
50 MHz	Port 2	_____	≤ 6°	N/A
1 GHz	Port 2	_____	≤ 6°	N/A
2 GHz	Port 2	_____	≤ 6°	N/A
3 GHz	Port 2	_____	≤ 6°	N/A
4 GHz	Port 2	_____	≤ 7.5°	N/A
5 GHz	Port 2	_____	≤ 7.5°	N/A
6 GHz	Port 2	_____	≤ 7.5°	N/A
50 MHz	Port 1	_____	≤ 6°	N/A
1 GHz	Port 1	_____	≤ 6°	N/A
2 GHz	Port 1	_____	≤ 6°	N/A
3 GHz	Port 1	_____	≤ 6°	N/A
4 GHz	Port 1	_____	≤ 7.5°	N/A
5 GHz	Port 1	_____	≤ 7.5°	N/A
6 GHz	Port 1	_____	≤ 7.5°	N/A

HP 87533 Performance Test Record (14 of 14)
For 30 kHz—6 GHz Analyzers

Hewlett-Packard Company **Model HP 8753E Option 006** **Serial Number** _____	**Report Number** _____ **Date** _____

▶▶ 17. Output/Input Test Port Harmonics (Option 002 only)

Test Description	Specification	Measurement Value	Measurement
Port output Harmonics			
Port 1 Input Harmonics			
Port 2 Input Harmonics			

		(dBc)	(dBc)	Uncertainty	

			(dB)
Test			
2nd	≤ 25	———	± 1.5
3rd	≤ 25	———	± 1.5
2nd	≤ 15	———	± 1.5
3rd	≤ 30	———	± 1.5
2nd	≤ 15	———	± 1.5
3rd	≤ 30	———	± 1.5

4

Start Troubleshooting Here

The information in this chapter helps you:

- Identify the portion of the analyzer that is at fault.
- Locate the specific troubleshooting procedures to identify the assembly or peripheral at fault.

To identify the portion of the analyzer at fault, follow these procedures:

Step 1. Initial Observations

Step 2. Operator's Check

Step 3. HP-IB Systems Check

Step 4 Faulty Group Isolation

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 87533 network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Having Your Analyzer Serviced

The HP 8753E has a one year on-site warranty, where available. If the analyzer should fail any of the following checks, call your local HP sales or service office. A customer engineer will be dispatched to service your analyzer on-site. If a customer engineer is not available in your area, follow the steps below to send your analyzer back to HP for repair.

1. Choose the nearest HP service center. (A table listing of Hewlett-Packard sales or service offices is provided at the end of this guide.)
2. Include a detailed description of any failed test and any error message.
3. Ship the analyzer, using the original or comparable antistatic packaging materials.

Step 1. Initial Observations

Initiate the Analyzer Self-Test

1. Disconnect all devices and peripherals from the analyzer.
2. Switch on the analyzer and press (Preset).
3. Watch for the indications shown in Figure 4-1 to determine if the analyzer is operating correctly.

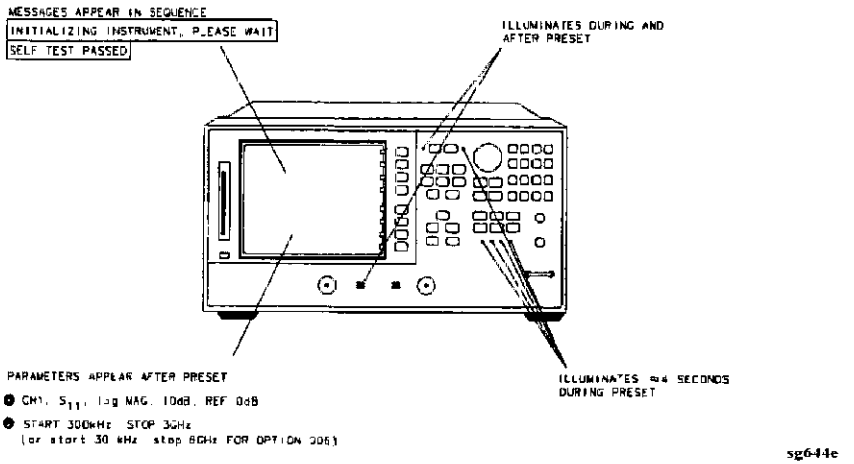


Figure 4-1. Preset Sequence

- If the self-test failed, refer to "Step 4. Faulty Group Isolation".

Step 2. Operator's Check

Description

The operator's check consists of two softkey initiated tests: Port 1 Op Chk and Port 2 Op Chk

A short is connected to port 1 (port 2) to reflect all the source energy back into the analyzer for an S_{11} (S_{22}) measurement.

The first part of Port 1 Op Chk checks the repeatability of the transfer switch. An S_{11} measurement is stored in memory and the switch is toggled to port 2 and then back to port 1 where another S_{11} measurement is made. The difference between the memory trace and the second trace is switch repeatability.

The remaining parts of both tests exercise the internal attenuator in 5 dB steps over a 55 dB range.

The resulting measurements must fall within a limit testing window to pass the test. The window size is based on both source and receiver specifications.

The operator's check determines that:

- The source is phase locked across the entire frequency range.
- All three samplers are functioning properly.
- The transfer switch is operational
- The attenuator steps 5 dB at a time.

Required Equipment and Tools

Short.....part of the HP 85031B calibration kit

Analyzer warm-up time: **30 minutes.**

Procedure

1. Disconnect all devices, peripherals, and accessories (including adapters and limiters) from the analyzer.
2. To run the test for port 1, press **[Preset] [PRESET: FACTORY] [System] [SERVICE MENU] [TESTS] [EXTERNAL TESTS].**
3. The display should show TEST 21 Port 1 Op Chk in the active entry area.

4. Press **[EXECUTE TEST]** to begin the test.

5. At the prompt, connect the short to the port indicated. Make sure the connection is tight.

6. Press **[CONTINUE].**

7. The test is a sequence of subtests. At the end of the subtests, the test title and result will be displayed. If all tests pass successfully, the overall test status will be PASS. If any test fails, the overall test status will be FAIL.

8. To run the test for port 2, press the step ⇧ key. The display should show TEST 22 Port 2 Op Chk in the active entry area.

9. Repeat steps 4 through 7.

10. If both tests pass, the analyzer is about 80% verified. If either test fails, refer to "Step 4. Faulty Group Isolation" in this section, or:

    a. Make sure that the connection is tight. Repeat the test.

    b. Visually inspect the connector interfaces and clean if necessary (refer to "Principles of Microwave Connector Care" located in Chapter 1).

    c. Verify that the short meets published specifications.

    d. Substitute another short, and repeat the test.

    e. Finally, refer to the detailed tests located in this section, or fault isolation procedures located in the troubleshooting sections.

Step 3. HP-IB Systems Check

Check the analyzer's HP-IB functions with a *known working* passive peripheral (such as a plotter, printer, or disk drive).

1. Connect the peripheral to the analyzer using a good HP-IB cable.
2. Press **[Local] [SYSTEM CONTROLLER]** to enable the analyzer to control the peripheral.
3. Then press **[SET ADDRESSES]** and the appropriate softkeys to verify that the device addresses will be recognized by the analyzer. The factory default addresses are:

Device	HP-IB Address
HP 8753E	16
Plotter port - HP-IB	5
Printer port - HP-IB	1
Disk (external)	0
Controller	21
Power meter - HP-IB	13

Note

You may use other addresses with two provisions:

- Each device must have its own address.
- The address set on each device must match the one recognized by the analyzer (and displayed).

Peripheral addresses are often set with a rear panel switch Refer to the manual of the peripheral to read or change its address.

If Using a Plotter or Printer

1. Ensure that the plotter or printer is set up correctly:
   - Power is on.
   - Pens and paper loaded.
   - Pinch wheels are down.
   - Some plotters need to have P1 and P2 positions set.
2. Press **[Copy]** and then **[PLOT]** or **[PRINT MONOCHROME.**
   - If the result is a copy of the analyzer display, the printing/plotting features are functional in the analyzer. Continue with "Troubleshooting Systems with Multiple Peripherals", "Troubleshooting Systems with Controllers", or the "Step 4. Faulty Group Isolation" section in this chapter.

     If the result is not a copy of the analyzer display, suspect the HP-IB function of the analyzer. Refer to Chapter 6, "Digital Control Troubleshooting."

If Using an External Disk Drive

1. Select the external disk drive. Press **[Save/Recall] [SELECT DISK] [EXTERNAL DISK].**
2. Verify that the address is set correctly. Press **[Local] [SET ADDRESSES] [ADDRESS: DISK].**
3. Ensure that the disk drive is set up correctly:
   - Power is on.
   - An initialized disk in the correct drive.
   - Correct disk unit number and volume number (press **[Local]** to access the softkeys that display the numbers; default is 0 for both).
   - With hard disk (Winchester) drives, make sure the configuration switch is properly set (see drive manual).

4. Press **[Start] [1] [M/μ] [Save/Recall] [SAVE STATE].** Then press **[Preset] [Save/Recall] [RECALL STATE].**

   - If the resultant trace starts at 1 MHz, HP-IB is functional in the analyzer. Continue with "Troubleshooting Systems with Multiple Peripherals", "Troubleshooting Systems with Controllers", or the "Step 4. Faulty Group Isolation" section in this chapter.
   - If the resultant trace does not start at 1 MHz, suspect the HP-IB function of the analyzer: refer to Chapter 6, "Digital Control Troubleshooting"

Troubleshooting Systems with Multiple Peripherals

Connect any other system peripherals (but not a controller) to the analyzer one at a time and check their functionality. Any problems observed are in the peripherals, cables, or are address problems (see above).

Troubleshooting Systems with Controllers

Passing the preceding checks indicates that the analyzer's peripheral functions are normal. Therefore, if the analyzer has not been operating properly with an external controller, check the following:

- The HP-IB interface hardware is incorrectly installed or not operational. (See "HP-1B Requirements" in the *HP 8753E Network Analyzer User's Guide.)*
- The programming syntax is incorrect (Refer to the *HP 8753E Network Analyzer Programmer's Guide.)*

If the analyzer appears to be operating unexpectedly but has not completely failed, go to "Step 4. Faulty Group Isolation."

Step 4. Faulty Group Isolation

Use the following procedures only if you have read the previous sections in this chapter and you think the problem is in the analyzer. These are simple procedures to verify the four functional groups in sequence, and determine which group is faulty.

The four functional groups are:

- power supplies
- digital control
- source
- receiver

Descriptions of these groups are provided in Chapter 12, "Theory of Operation."

The checks in the following pages must be performed in the order presented. If one of the procedures fails, it is an indication that the problem is in the functional group checked. Go to the troubleshooting information for the indicated group, to isolate the problem to the defective assembly.

Figure 4-2 illustrates the troubleshooting organization.

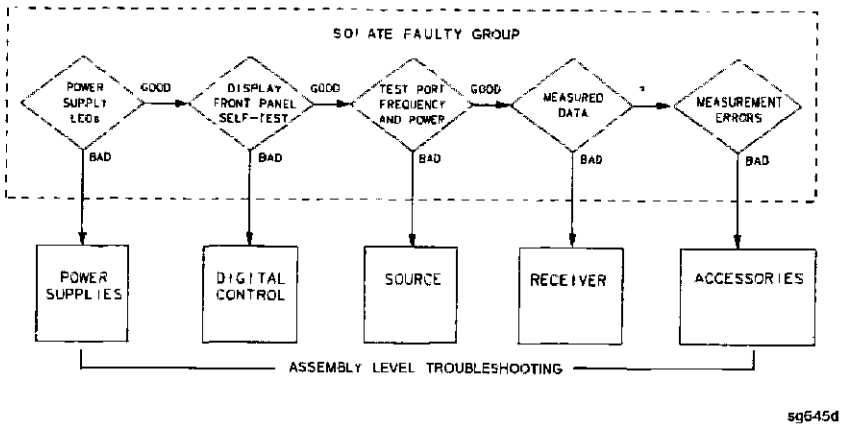


Figure 4-2. Troubleshooting Organization

Power Supply

Check the Rear Panel LEDs

Switch on the analyzer. Notice the condition of the two LEDs on the A15 preregulator at rear of the analyzer. (See Figure 4-3.)

- The upper (red) LED should be off.
- The lower (green) LED should be on.

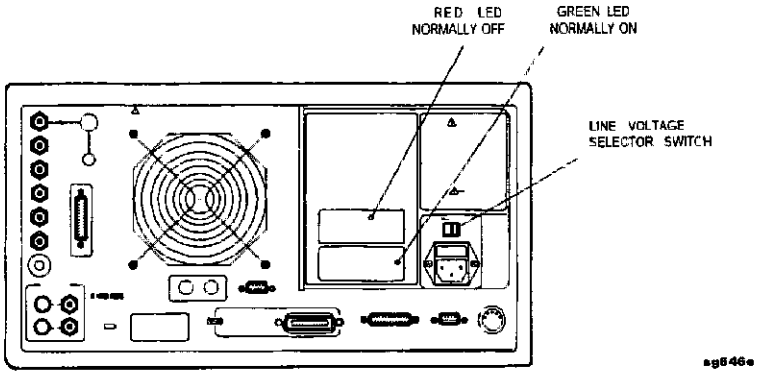


Figure 4-3. A15 Preregulator LEDs

Check the A8 Post Regulator LEDs

Remove the analyzer's top cover. Switch on the power. Inspect the green LEDs along the top edge of the A8 post-regulator assembly.

- All green LEDs should be on.
- The fan should be audible.

In case of difficulty, refer to Chapter 5, "Power Supply Troubleshooting."

Digital Control

Observe the Power Up Sequence

Switch the analyzer power off, then on. The following should take place within a few seconds:

- On the front panel, observe the following:
  1. All six amber LEDs illuminate.
  2. The port 2 LED illuminates.
  3. The amber LEDs go off after a few seconds, except the CH 1 LED. At the same moment, the port 2 LED goes off and the port 1 LED illuminates. (See Figure 4-4.)
- The display should come up bright with no irregularity in colors.
- After an initial pattern, five red LEDs on the A9 CPU board should remain off. They can be observed through a small opening in the rear panel.

If the power up sequence does not occur as described, or if there are problems using the front panel keyboard, refer to Chapter 6, "Digital Control Troubleshooting."

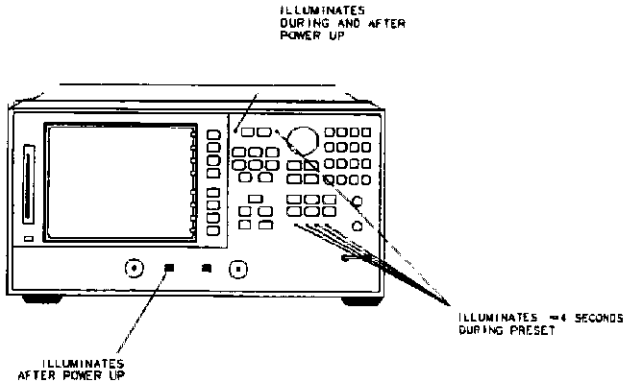


Figure 4-4. Front Panel Power Up Sequence

Verify Internal Tests Passed

1. Press **[Preset] [System] [SERVICE MENU] [TESTS] [INTERNAL TESTS] [EXECUTE TEST]**. The display should indicate:

   TEST

   0 ALL INT PASS

   - If your display shows the above message, go to step 2. Otherwise, continue with this step.
   - If phase lock error messages are present, this test may stop without passing or failing. In this case, continue with the next procedure to check the source.
   - If you have unexpected results, or if the analyzer indicates a specific test failure, that internal test (and possibly others) have failed; the analyzer reports the first failure detected. Refer to Chapter 6, "Digital Control Troubleshooting."
   - If the analyzer indicates failure but does not identify the test, press ⇧ to search for the failed test. Then refer to Chapter 6, "Digital Control Troubleshooting. ' Likewise, if the response to front panel or HP-IB commands is unexpected, troubleshoot the digital control group.

2. Perform the Analog Bus test Press **[RETURN] [19] [x1] [EXECUTE TEST].**

   - If this test fails, refer to Chapter 6, "Digital Control Troubleshooting."
   - If this test passes, continue with the next procedure to check the source.

Source

Phase Lock Error Messages

The error messages listed below are usually indicative of a source failure or improper instrument configuration. (Ensure that the R channel input is receiving at least -35 dBm power). Continue with this procedure.

- **NO IF FOUND: CHECK R INPUT LEVEL**

  The first IF was not detected during the pretune stage of phase lock.

- **NO PHASE LOCK: CHECK R INPUT LEVEL**

  The first IF was detected at the pretune stage but phase lock could not be acquired thereafter.

- **PHASE LOCK LOST**

  Phase lock was acquired but then lost.

- **PHASE LOCK CAL FAILED**

  An internal phase lock calibration routine is automatically executed at power-on, when pretune values drift, or when phase lock problems are detected. A problem spoiled a calibration attempt.

- **POSSIBLE FALSE LOCK**

  The analyzer is achieving phase lock but possibly on the wrong harmonic comb tooth.

- **SWEEP TIME TOO FAST**

  The fractional-N and the digital IF circuits have lost synchronization.

Check Source Output Power

1. Connect the equipment as shown in Figure 4-5. Be sure that any special accessories, such as limiters, have been disconnected.

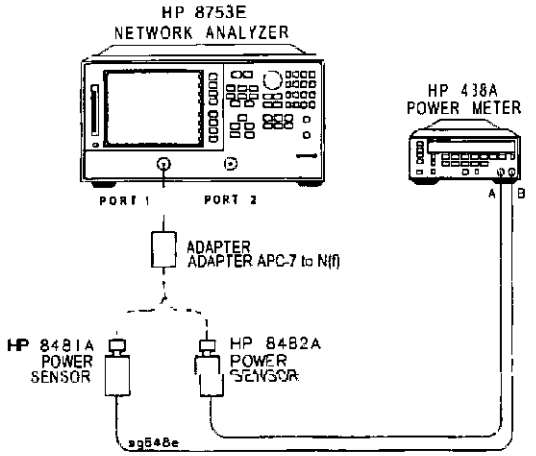


Figure 4-5. Equipment Setup for Source Power Check

2. Zero and calibrate the power meter. Press **[Preset]** on the analyzer to initialize the instrument.
3. On the analyzer, press **[Menu] [CW FREQ] [300] [k/m]** to output a CW 300 signal. The power meter should read approximately 0 dBm.
4. Press **[16] [M/μ]** to change the CW frequency to 16 MHz. The output power should remain approximately 0 dBm throughout the analyzer frequency range. Repeat this step at 1 and 3 GHz (For Option 006 include an additional check at 6 GHz.)

If any incorrect power levels are measured, refer to Chapter 7, "Source Troubleshooting."

No Oscilloscope or Power Meter? Try the ABUS

Monitor ABUS node 16.

1. Press **[Preset] [Start] [300] [k/m] [Stop] [3] [G/n] [System] [SERVICE MENU] [ANALOG BUS ON].**

2. (Meas) **ANALOG IN Aux Input** (16) (x1).

3. **[Format] [MORE] [REAL] [Scale Ref] [AUTOSCALE].**

The display should resemble Figure 4-6.

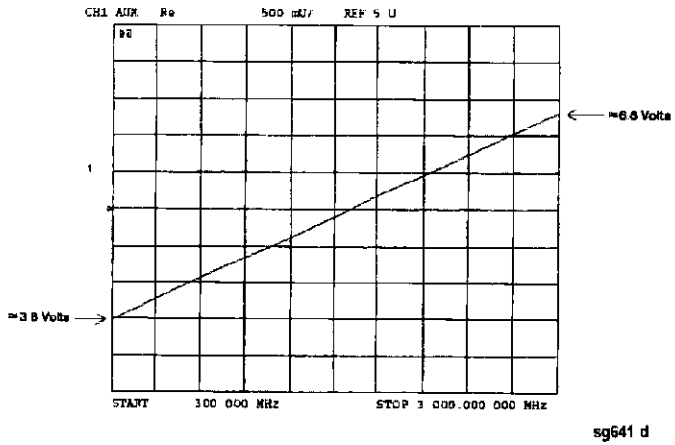


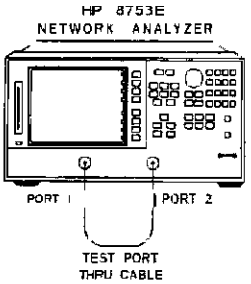
Figure 4-6. ABUS Node 16: 1 V/GHz

If any of the above procedures provide unexpected results, or if error messages are present, refer to Chapter 7, "Source Troubleshooting."

Receiver

Observe the A and B Input Traces

1. Connect the equipment as shown in Figure 4-7 below. Be sure that any special accessories, such as limiters, have been disconnected. (The through cable is HP part number 8120-4779.)



sg649e

Figure 4-7. Equipment Setup

2. Press **[Preset] [Meas] [INPUT PORTS] [A] [TEST PORT 2] [Scale Ref] [AUTO SCALE]**
3. Observe the measurement trace displayed by the A input The trace should have about the same flatness as the trace in Figure 4-8.
4. Press **[Meas] [INPUT PORTS] [TEST PORT 1] [B].**
5. Observe the measurement trace displayed by the B input. The trace should have about the same flatness as the trace in Figure 4-8.

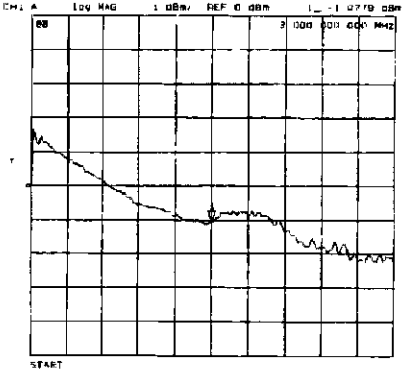


Figure 4-8. Typical Measurement Trace

If the source is working, but the A or B input traces appear to be in error, refer to Chapter 8, "Receiver Troubleshooting."

The following symptoms may also indicate receiver failure.

Receiver Error Messages

- **CAUTION: OVERLOAD ON INPUT A; POWER REDUCED**
- **CAUTION: OVERLOAD ON INPUT B; POWER REDUCED**
- **CAUTION: OVERLOAD ON INPUT R; POWER REDUCED**

The error messages above indicate that you have exceeded approximately + 14 dBm at one of the test ports. The RF output power is automatically reduced to -85 dBm. The annotation P↓ appears in the left margin of the display to indicate that the power trip function has been activated. When this occurs, press **[Menu] [POWER]** and enter a lower power level. Press **[SOURCE PWR ON]** to switch on the power again.

Faulty Data

Any trace data that appears to be below the noise floor of the analyzer (-100 dBm) is indicative of a receiver failure.

Accessories

If the analyzer has passed all of the previous checks but is still making incorrect measurements, suspect the system accessories. Accessories such as RF or interconnect cables, calibration or verification kit devices, limiters, and adapters can all induce system problems.

Reconfigure the system as it is normally used and reconfirm the problem. Continue with Chapter 9, "Accessories Troubleshooting."

Accessories Error Messages

- POWER PROBE SHUT DOWN!

  The biasing supplies to a front panel powered device (like a probe or millimeter module) are shut down due to excessive current draw. Troubleshoot the device.

5

Power Supply Troubleshooting

Use this procedure only if you have read Chapter 4, "Start Troubleshooting Here." Follow the procedures in the order given, unless:

- an error message appears on the display, refer to "Error Messages" near the end of this chapter.
- the fan is not working; refer to "Fan Troubleshooting" in this chapter.

The power supply group assemblies consist of the following:

- A8 post regulator
- A15 preregulator

All assemblies, however, are related to the power supply group because power is supplied to each assembly.

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 8753E network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Simplified Block Diagram

Figure 5-1 shows the power supply group in simplified block diagram form. Refer to the detailed block diagram of the power supply (Figure 5-8) located at the end of this chapter to see voltage lines and specific connector pin numbers.

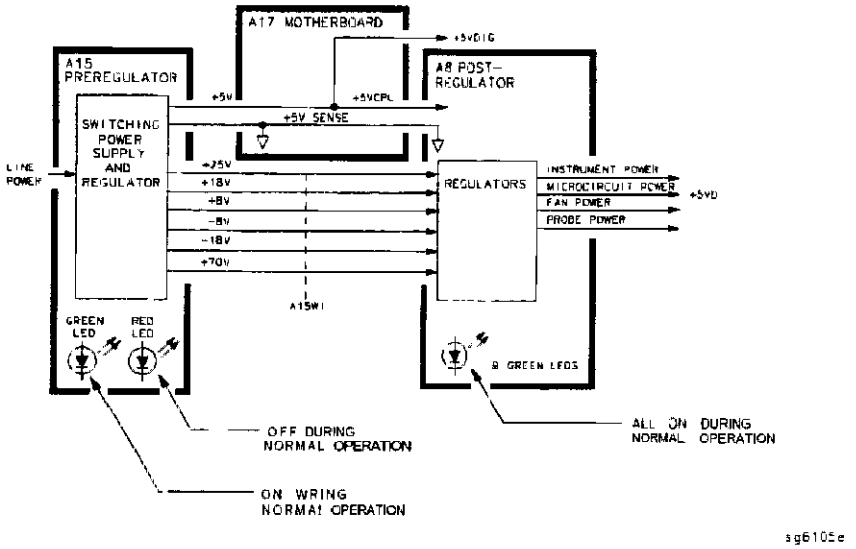


Figure 5-1. Power Supply Group Simplified Block Diagram

Start Here

Check the Green LED and Red LED on A15

Switch on the analyzer and look at the rear panel of the analyzer Check the two power supply diagnostic LEDs on the A15 preregulator casting by looking through the holes located to the left of the line voltage selector switch. (See Figure 5-2.)

During normal operation, the bottom (green) LED is on and the top (red) LED is off. If these LEDs are normal, then A15 is 95% verified. Continue to "Check the Green LEDs on A8".

- If the green LED is not on steadily, refer to "If the Green LED of the A15 Is not ON Steadily" in this procedure.
- If the red LED is on or flashing, refer to "If the Red LED of the A15 is ON" in this procedure.

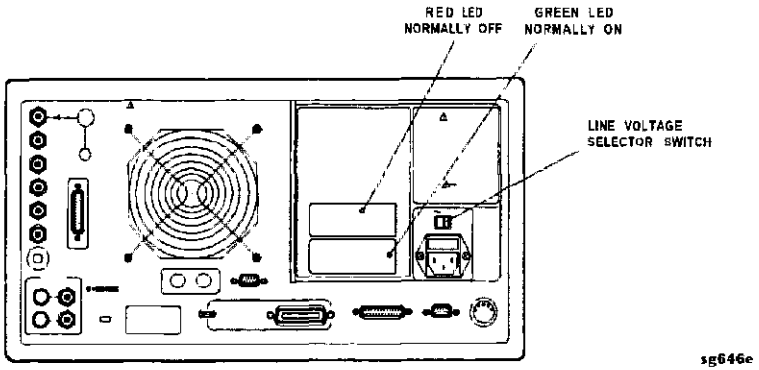


Figure 5-2. Location of A15 Diagnostic LEDs

Check the Green LEDs on A8

Remove the top cover of the analyzer and locate the A8 post regulator; use the location diagram under the top cover if necessary. Check to see if the green LEDs on the top edge of A8 are all on. There are nine green LEDs (one is not visible without removing the PC board stabilizer)

- If all of the green LEDs on the top edge of A8 are on, there is a 95% confidence level that the power supply is verified To confirm the last 5% uncertainty of the power supply, refer to "Measure the Post Regulator Voltages" (next).
- If any LED on the A8 post regulator is off or flashing, refer to "If the Green LEDs of the A8 are not All ON" in this procedure.

Measure the Post Regulator Voltages

Measure the DC voltages on the test points of A8 with a voltmeter. Refer to Figure 5-3 for test point locations and Table 5-1 for supply voltages and limits.

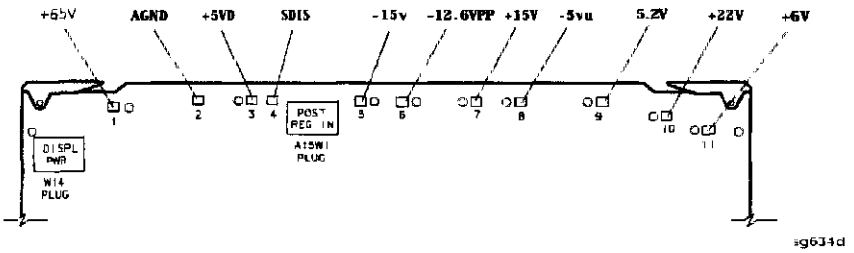


Figure 5-3. A8 Post Regulator Test Point Locations

Table 5-1. A8 Post Regulator Test Point Voltages

TP	Supply	Range
1	+66 V (not used)	+64.6 to +65.4
2	AGND	n/a
3	+5 VD	+4.9 to +5.3
4	SDIS	n/a
5	-15 V	-14.4 to -16.6
6	-12.6 VPP (probe power)	-12.1 to -12.8
7	+15 V	+14.5 to +15.5
8	+5 VU	+5.06 to +5.36
9	-6.2 V	-6.0 to -5.4
10	+22 V	+21.3 to +22.7
11	+6 V	+5.8 to +6.2

If the Green LED of the A15 Is not ON Steadily

If the green LED is not on steadily, the line voltage is not enough to power the analyzer.

Check the Line Voltage, Selector Switch, and Fuse

Check the main power line cord, line fuse, line selector switch setting, and actual line voltage to see that they are all correct. Figure 5-4 shows how to remove the line fuse, using a small flat-blade screwdriver to pry out the fuse holder. Figure 5-2 shows the location of the line voltage selector switch. Use a small flat-blade screwdriver to select the correct switch position.

If the A15 green LED is still not on steadily, replace A15.

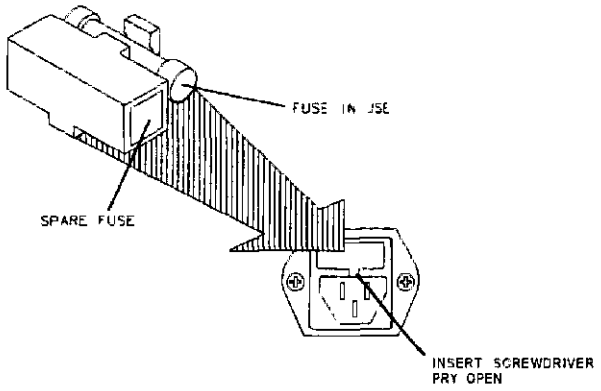


Figure 5-4. Removing the Line Fuse

If the Red LED of the A15 is ON

If the red LED is on or flashing, the power supply is shutting down. Use the following procedures to determine which assembly is causing the problem.

Check the A8 Post Regulator

1. Switch off the analyzer.
2. Disconnect the cable A15W1 from the A8 post regulator. (See Figure 5-5.)
3. Switch on the analyzer and observe the red LED on A15.
   - If the red LED goes out, the problem is probably the A8 post regulator. Continue to "Verify the A15 Preregulator" to first verify that the inputs to A8 are correct.
   - If the red LED is still on, the problem is probably the A15 preregulator, or one of the assemblies obtaining power from it. Continue with "Check for a Faulty Assembly".

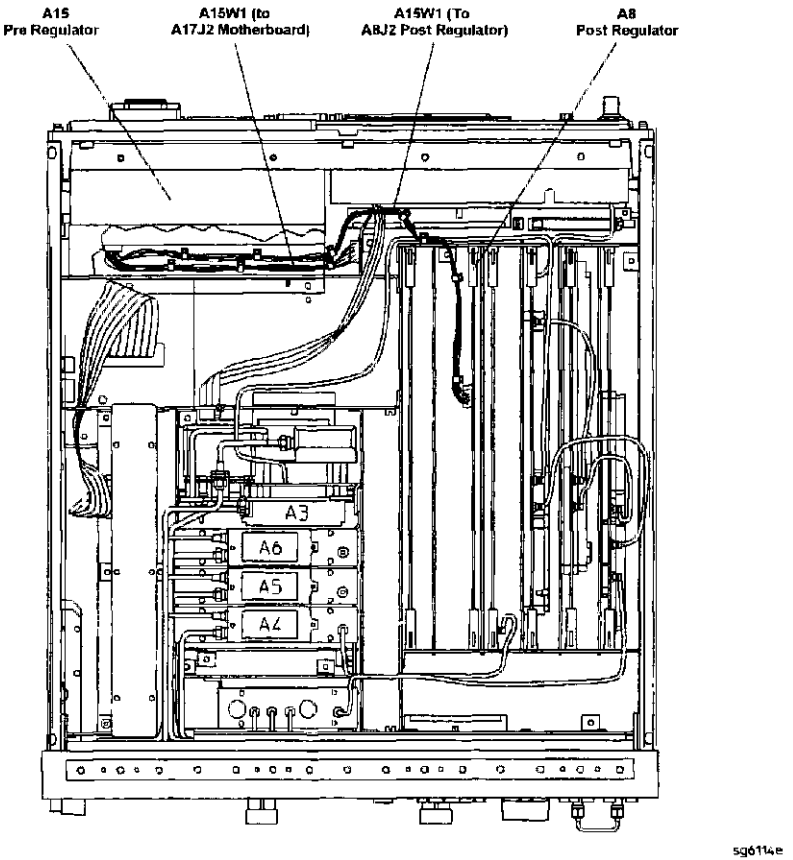


Figure 5-5. Power Supply Cable Locations

Verify the A15 Preregulator

Verify that the A15 preregulator is supplying the correct voltages to the A8 post regulator. Use a voltmeter with a small probe to measure the output voltages of A15W1's plug. Refer to Table 5-2 and Figure 5-6.

- If the voltages are not within tolerance, replace A15.

- If the voltages are within tolerance, A15 is verified. Continue to "Check for a Faulty Assembly".

Table 5-2. Output Voltages

Pin	A15W1P1 (Disconnected) Voltages	A8J2 (Connected) Voltages	A15 Preregulator Label
1	N/C	+ 68 to + 72	N/C
2	+125 to +100	+ 68 to + 72	+70 v
3,4	+ 22.4 to +33.6	+ 17.0 to + 18.4	+18 V
5,6	-22.4 to -33.6	- 17.0 to - 18.4	-18 v
7	N/C	+7.4 to +8.0	N/C
8	+9.4 to +14	+7.4 to +8.0	+8 V
9,10	-9.4 to -14	-6.7 to -7.3	- 8 V
11	N/C	+24.6 to +28.6	N/C
12	+32 to + 48	+24.6 to +28.6	+25 V

NOTE The + 6 VD supply must be loaded by one or more assemblies at all times, or the other voltages will not be correct. It connects to the motherboard connector A17J3 Pin 4.

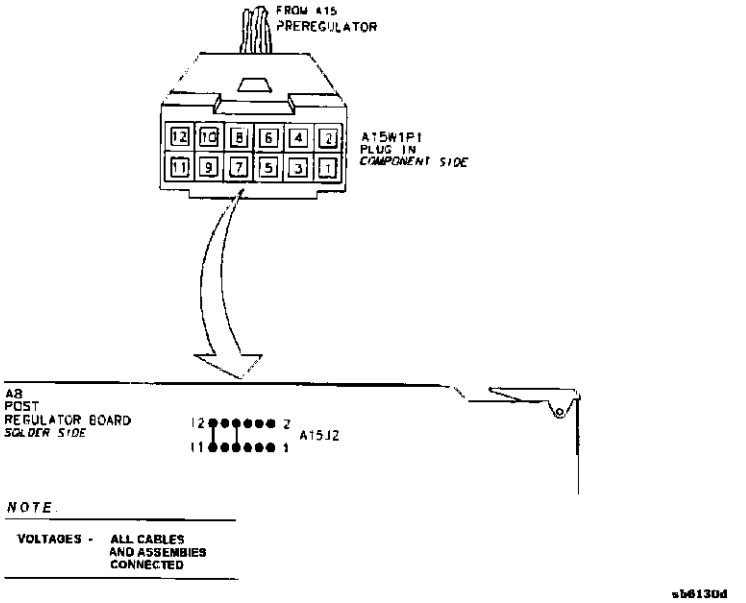


Figure 5-6. A15W1 Plug Detail

Check for a Faulty Assembly

This procedure checks for a faulty assembly that might be shutting down the A15 preregulator via one of the following lines (also refer to Figure 5-1):

- A15W1 connecting to the A8 post regulator
- the +5VCPU line through the motherboard
- the +5VDIG line through the motherboard

Do the following:

1. Switch off the analyzer.
2. Ensure that A15W1 is reconnected to A8. (Refer to Figure 5-5.)
3. Remove or disconnect the assemblies listed in Table 5-3 one at a time and in the order shown. The assemblies are sorted from most to least accessible. Table 5-3 also lists any associated assemblies that are supplied

by the assembly that is being removed. After each assembly is removed or disconnected switch on the analyzer and observe the red LED on A15.

Note ***Always switch off the analyzer before removing or disconnecting assemblies.***

- When extensive disassembly is required, refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
- Refer to Chapter 13, "Replaceable Parts," to identify specific cables and assemblies that are not shown in this chapter.

- If the red LED goes out, the particular assembly (or one receiving power from it) that allows it to go out is faulty.
- If the red LED is still on after you have checked all of the assemblies listed in Table 5-3, continue to "Check the Operating Temperature".

Table 5-3. Recommended Order for Removal/Disconnection

Assembly To Remove	Removal or Disconnection Method	Other Assemblies that Receive Power from the Removed Assembly
1. A19 Graphics Processor	Remove from Card Cage	None
2. A14 Frac N Digital	Remove from Card Cage	None
8. A9 CPU	Disconnect W36	A20 Disk Drive
4. A16 Rear Panel Interface	Disconnect W27	A25 Test Set Interface A24 Transfer Switch A23 LED Front Panel
5. A2 Front Panel Interface	Disconnect W17	A1 Front Panel Keyboard A18 Display

Check the Operating Temperature

The temperature sensing circuitry inside the A15 preregulator may be shutting down the supply. Make sure the temperature of the open air operating environment does not exceed 55°C (131°F), and that the analyzer fan is operating.

- If the fan does not seem to be operating correctly, refer to "Fan Troubleshooting" at the end of this procedure.
- If there does not appear to be a temperature problem, it is likely that A15 is faulty.

Inspect the Motherboard

If the red LED is still on after replacement or repair of A15, switch off the analyzer and inspect the motherboard for solder bridges and other noticeable defects. Use an ohmmeter to check for shorts. The +5 VD, +5 VCPU, or +5 VDSENSE lines may be bad. Refer to the bloek diagram (Figure 5-8) at the end of this chapter and troubleshoot these suspected power supply lines on the A17 motherboard

If the Green LEDs of the A8 are not All ON

The green LEDs along the top edge of the A8 post regulator are normally on.

Flashing LEDs on A8 indicate that the shutdown circuitry on the A8 post regulator is protecting power supplies from overcurrent conditions by repeatedly shutting them down. This may be caused by supply loading on A8 or on any other assembly in the analyzer.

Remove A8, Maintain A15W1 Cable Connection

1. Switch off the analyzer.
2. Remove A8 from its motherboard connector, but keep the A15W1 cable connected to A8.
3. Short A8TP2 (AGND) (see Figure 5-3) to chassis ground with a clip lead.
4. Switch on the analyzer and observe the green LEDs on A8.
   - If any green LEDs other than +5 VD are still off or flashing, continue to "Check the A8 Fuses and Voltages".
   - If all LEDs are now on steadily except for the +5 VD LED, the A15 preregulator and A8 post regulator are working properly and the trouble is excessive loading somewhere after the motherboard connections at A8. Continue to "Remove the Assemblies".

Check the A8 Fuses and Voltages

Check the fuses along the top edge of A8. If any A8 fuse has burned out, replace it. If it burns out again when power is applied to the analyzer, A8 or A15 is faulty. Determine which assembly has failed as follows.

1. Remove the A15W1 cable at A8. (See Figure 5-5.)
2. Measure the voltages at A15W1P1 (see Figure 5-6) with a voltmeter having a small probe.
3. Compare the measured voltages with those in Table 5-2.
   - If the voltages are within tolerance, replace A8.
   - If the voltages are not within tolerance, replace A15.

If the green LEDs are now on, the A15 preregulator and A8 post regulator are working properly and the trouble is excessive loading somewhere after the motherboard connections at A8. Continue to "Remove the Assemblies".

Remove the Assemblies

1. Switch off the analyzer.
2. Install A8. Remove the jumper from A8TP2 (AGND) to chassis ground.
3. Remove or disconnect all the assemblies listed below. (See Figure 5-5.)
   Always switch off the analyzer before removing or disconnecting an assembly.

   A10 digital IF
   A11 phase lock
   A12 reference
   A13 fractional-N analog
   A14 fractional-N digital
   A19 graphics processor
4. Switch on the analyzer and observe the green LEDs on A8.
   - If any of the green LEDssare off or flashing, it is not likely that any of the assemblies listed above is causing the problem. Continue to "Briefly Disable the Shutdown Circuitry".
   - If all green LEDs are now on, one or more of the above assemblies may be faulty. Continue to next step.
5. Switch off the analyzer.
6. Reinstall each assembly one at a time. Switch on the analyzer after each assembly is installed. The assembly that causes the green LEDs to go off or flash could be faulty.

Note It is possible, however, that this condition is caused by the A8 post regulator not supplying enough current. To check this, reinstall the assemblies in a different order to change the loading. If the same assembly appears to be faulty, replace that assembly. If a different assembly appears faulty, A8 is most likely faulty (unless both of the other assemblies are faulty).

Briefly Disable the Shutdowu Circuitry

In this step, you shutdown the protective circuitry for a short time, and the supplies are forced on (including shorted supplies) with a 100% duty cycle.

Caution Damage to components or to circuit traces may occur if A8TP4 (SDIS) is shorted to chassis ground for more than a few seconds while supplies are shorted.

1. Connect A8TP4 (SDIS) to chassis ground with a jumper wire.
2. Switch on the analyzer and note the signal mnemonics and test points of any LEDs that are off. *Immediately remove the jumper wire.*
3. Refer to the block diagram (Figure 5-8) at the end of this chapter and do the following:
   - Note the mnemonics of any additional signals that may connect to any A8 test point that showed a fault in the previous step.
   - Cross reference all assemblies that use the power supplies whose A8 LEDs went out when A8TP4 (SDIS) was connected to chassis ground.

- Make a list of these assemblies.
- Delete the following assemblies from your list as they have already been verified earlier in this section

  A10 digital IF
  A11 phase lock
  A12 reference
  A13 fractional-N analog
  A14 fractional-N digital
  A19 graphics processor

4. Switch off the analyzer.
5. Of those assemblies that are left on the list, remove or disconnect them from the analyzer one at a time. Table 5-4 shows the best order in which to remove them, sorting them from most to least accessible. Table 5-4 also lists any associated assemblies that are supplied by the assembly that is being removed. After each assembly is removed or disconnected, switch on the analyzer and observe the LEDs.

Note

- *Always switch off the analyzer before removing or disconnecting assemblies.*
- When extensive disassembly is required, refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
- Refer to Chapter 13, "Replaceable Parts", to identify specific cables and assemblies that are not shown in this chapter.

- If all the LEDs light, the assembly (or one receiving power from it) that allows them to light is faulty.
- If the LEDs are still not on steadily, continue to "Inspect the Motherboard".

Table 5-4. Recommended Order for Removal/Disconnection

Assembly To Remove	Removal or Disconnection Method	Other Assemblies that Receive Power from the Removed Assembly
1. A3 Source	Remove from Card Cage	None
2. A7 Pulse Generator	Remove from Card Cage	None
3. A4 R Sampler	Remove from Card Cage	None
4. A5 A Sampler	Remove from Card Cage	None
5. A6 B Sampler	Remove from Card Cage	None
6. A9 CPU	Disconnect W35 and W36	A20 Disk Drive
7. A2 Front Panel Interface	Disconnect W17	Al Front Panel Keyboard
8. Al6 Rear Panel Interface	Disconnect W27	A25 Test Set Interface A24 Transfer Switch A23 LED Front Panel

Inspect the Motherboard

Inspect the Al7 motherboard for solder bridges and shorted traces. In particular, inspect the traces that carry the supplies whose LEDs faulted when A8TP4 (SDIS) was grounded earlier.

Error Messages

Three error messages are associated with the power supplies functional group. They are shown here.

- **POWER SUPPLY SHUT DOWN!**

  One or more supplies on the A8 post regulator assembly is shut down due to one of the following conditions: overcurrent, overvoltage, or undervoltage. Refer to "If the Red LED of the A15 is ON" earlier in this procedure.

- **POWER SUPPLY HOT**

  The temperature sensors on the A8 post regulator assembly detect an overtemperature condition. The regulated power supplies on A8 have been shut down.

  Check the temperature of the operating environment; it should not be greater than +55°C (131°F). The fan should be operating and there should be at least 15 cm (6 in) spacing behind and all around the analyzer to allow for proper ventilation.

- **PROBE POWER SHUT DOWN!**

  The front panel RF probe biasing supplies are shut down due to excessive current draw. These supplies are + 15 VPP and -12.6 VPP, both supplied by the A8 post regulator. + 15 VPP is derived from the + 15 V supply. -12.6 VPP is derived from the -12.6 V supply.

  Refer to Figure 5-7 and carefully measure the power supply voltages at the front panel RF probe connectors.

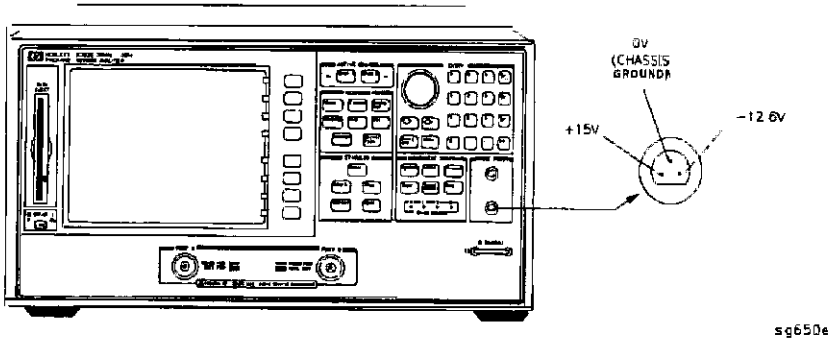


Figure 5-7. Front Panel Probe Power Connector Voltages

- If the correct voltages are present, troubleshoot the probe.
- If the voltages are not present, check the + 15 V and -12.6 V green LEDs on A8.
  - If the LEDs are on, there is an open between the A8 assembly and the front panel probe power connectors Put A8 onto an extender board and measure the voltages at the following pins:

A8P2	pins 6 and 36	-12.6 volts
A8P2	pins 4 and 34	+15 volts

  - If the LEDs are off, continue with "Check the Fuses and Isolate A8".

Check the Fuses and Isolate A8

Check the fuses associated with each of these supplies near the A8 test points. If these fuses keep burning out, a short exists. Try isolating A8 by removing it from the motherboard connector, but keeping the cable A15W1 connected to A8J2 Connect a jumper wire from A8TP2 to chassis ground. If either the +15 V or -12.6 V fuse blows, or the associated green LEDs do not light, replace A8.

If the +15 V and -12.6 V green LEDs light, troubleshoot for a short between the motherboard connector pins XA8P2 pins 6 and 36 (-12.6 V) and the front panel probe power connectors. Also check between motherboard connector pins XA8P2 pins 4 and 34 (+15 V) and the front panel probe power connectors.

Fan Troubleshooting

Fan Speeds

The fan speed varies depending upon temperature, It is normal for the fan to be at high speed when the analyzer is just switched on, and then change to low speed when the analyzer is cooled.

Check the Fan Voltages

If the fan is dead, refer to the A8 post regulator block diagram (Figure 5-8) at the end of this chapter. The fan is driven by the +18 V and -18 V supplies coming from the A15 preregulator. Neither of these supplies is fused.

The -18 V supply is regulated on A8 in the fan drive block, and remains constant at approximately -14 volts. It connects to the A17 motherboard via pin 32 of the A8P1 connector.

The +18 V supply is regulated on A8 but changes the voltage to the fan, depending on airflow and temperature information. Its voltage ranges from approximately -1.0 volts to + 14.7 volts, and connects to the A17 motherboard via pin 31 of the A8P1 connector.

Measure the voltages of these supplies while using an extender board to allow access to the PC board connector, A8P1.

Short A8TP3 to Ground

If there is no voltage at A8P1 pins 31 and 32, switch off the analyzer. Remove A8 from its motherboard connector (or extender board) but keep the cable A15W1 connected to A8. (See Figure 5-5.) Connect a jumper wire between A8TP3 and chassis ground. Switch on the analyzer.

- If all the green LEDs on the top edge of A8 light (except +5 VD), replace the fan.
- If other green LEDs on A8 do not light, refer to "If the Green LEDs of the A8 are not All ON" earlier in this procedure.

Intermittent Problems

PRESET states that appear spontaneously (without pressing **[Preset]** typically signal a power supply or A9 CPU problem. Since the A9 CPU assembly is the easiest to substitute, do so. If the problem ceases, replace the A9. If the problem continues, replace the A15 preregulator assembly.

6

Digital Control Troubleshooting

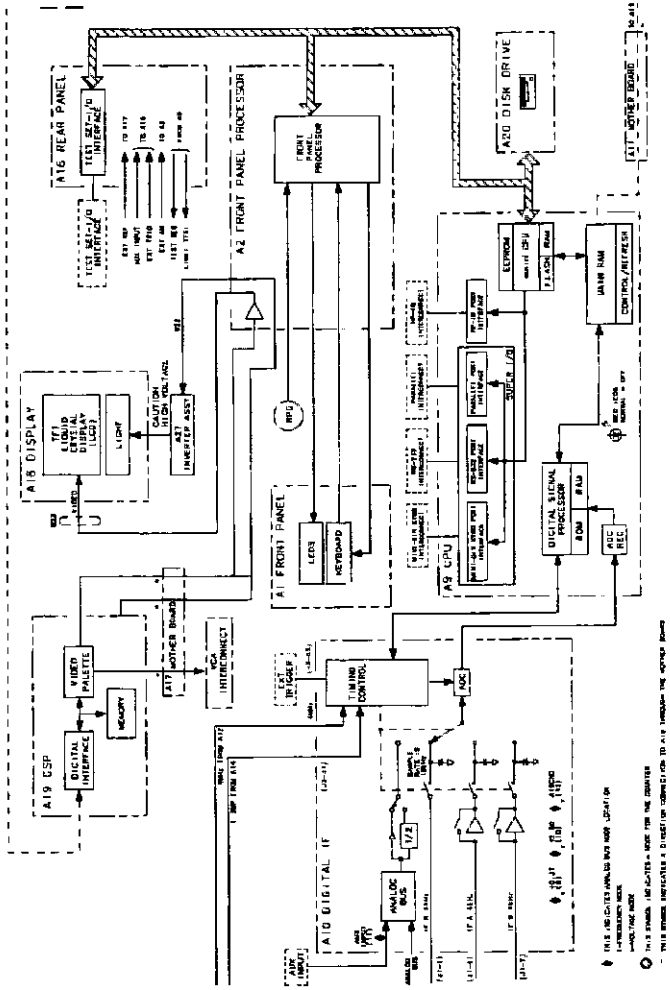
Use this procedure only if you have read Chapter 4, "Start Troubleshooting Here."

The digital control group assemblies consist of the following:

- CPU
  - A9
- Display
  - A2, A18, A19, A27
- Front Panel
  - A1, A2
- Digital IF
  - A10
- Rear Panel Interface
  - A16

Begin with "CPU Troubleshooting," then proceed to the assembly that you suspect has a problem. If you suspect an HP-IB interface problem, refer to "HP-IB Failures," at the end of this chapter.

Digital Control Group Block Diagram



sg6107e

Figure 6-1. Digital Control Group Block Diagram

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 8753E network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

CPU Troubleshooting (A9)

A9 CC Switch Positions

The A9 CC switch must be in the NORMAL position for these procedures. This is the position for normal operating conditions. To move the switch to the NORMAL position, do the following:

1. Remove the power line cord from the analyzer.
2. Set the analyzer on its side.
3. Remove the two corner bumpers from the bottom of the instrument with a T- 15 TORX screwdriver.
4. Loosen the captive screw on the bottom cover's back edge.
5. Slide the cover toward the rear of the instrument.
6. Move the switch to the NORMAL position as shown in Figure 6-2.
7. Replace the bottom cover and power cord.

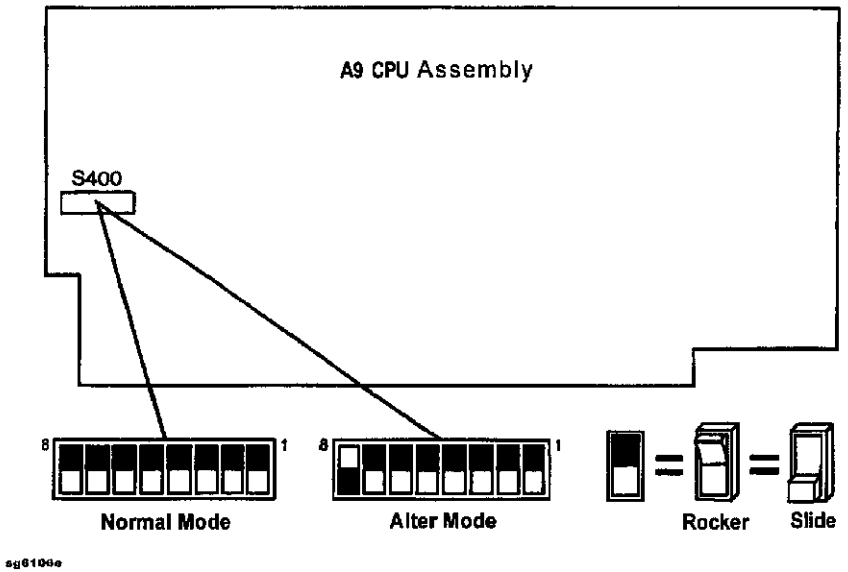


Figure 6-2. Switch Positions on the A9 CPU

Checking A9 CPU Red LED Patterns

The A9 CPU has five red LEDs that can be viewed through a small opening in the rear panel of the analyzer. (See Figure 6-3.) Four LEDs are easily viewable. The fifth LED must be viewed by looking to the left at an angle.

1. Cycle the power while observing five red LEDs

Cycle the power on the analyzer and observe the five red LEDs. After an initial pattern, the five red LEDs on the A9 CPU board should remain off

- If the LEDs remained off, then proceed to the assembly that you suspect has a problem.
- If the LEDs did not remain off, switch off the power and remove the bottom cover for further troubleshooting.

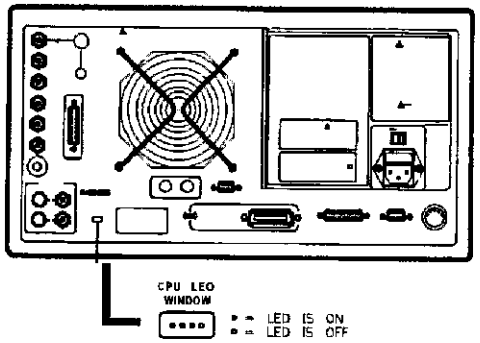


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Figure 6-3. CPU LED Window on Rear Panel

2. Cycle the power while observing all eight red LEDs

With the analyzer positioned bottom up, cycle the power and observe the eight red LEDs while looking from the front of the instrument.

Note If firmware did not load, a red LED on the CPU board will be flashing. Refer to "Loading Firmware" in Chapter 3.

---

3. Evaluate results

- If either of the following LED patterns remain, go to "Display Troubleshooting."

■ ■ ■ o ■ ■ ■ o

■ ■ ■ o ■ ■ o ■

(front of instrument ⇩)

- If any other LED patterns remain, replace the A9 CPU after verifying the power supply.

Display Troubleshooting (A2, A18, A19, A27)

This section contains the following information:

- Evaluating your Display
- Troubleshooting a White Display
- Troubleshooting a Black Display
- Troubleshooting a Display with Color Problems

Evaluating your Display

Switch the analyzer off, and then on. The display should be bright with the annotation legible and intelligible. There are four criteria against which your display is measured:

- Background Lamp Intensity
- Green, Red or Blue Stuck Pixels
- Dark Stuck Pixels
- Newtons Rings

Evaluate the display as follows:

- If either the A18 LCD, A19 GSP, A9 CPU or A27 backlight inverter assemblies are replaced, perform a visual inspection of the display.
- If it appears that there is a problem with the display, refer to the troubleshooting information that follows.
- If the new display appears dim or doesn't light, see "Backlight Intensity Check," next.

Backlight Intensity Check

Required Equipment and Tools

Photometer	Tektronix J16
Probe	Tektronix J6503
Light Occlude	Tektronix 016-0305-00
Antistatic Wrist Strap	HP P/N 9300-1367
Antistatic Wrist Strap Cord	HP P/N 9300-0980
Static-control Table Mat and Earth Ground Wire	HP P/N 9300-0797

Analyzer warm-up time: **30 minutes.** *Photometer warm-up time:* **30 minutes.**

Note This procedure should be performed with a photometer and only by qualified personnel.

---

1. Press **[Display] [MORE] [ADJUST DISLAY] [INTENSITY] [100] [x1],** to set the display intensity at 100%.
2. Press **[System] [SERVICE MENU] [TESTS] [62] [x1] [EXECUTE TEST] [CONTINUE],** to set a white screen test pattern on the display.
3. Set the photometer probe to NORMAL Press **[POWER]** on the photometer to switch it on and allow 30 minutes of warm-up time. Zero the photometer according to the manufacturer's instructions.
4. Center the photometer on the analyzer display as shown in Figure 6-4.

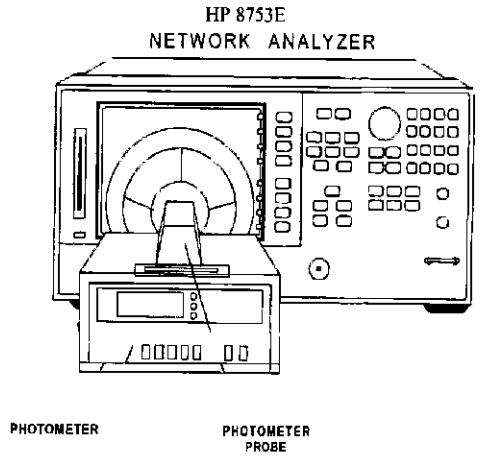


Figure 6-4. Backlight Intensity Check Setup

Note The intensity levels are read with a display bezel installed.

5. If the photometer registers less than 50 Nits, the display backlight lamp is bad. Refer to the "Replacement Procedures" chapter in the service manual for information on display lamp replacement.

Red, Green, or Blue Pixels Specifications

Red, green, or blue "stuck on" pixels may appear against a black background. To test for these dots, press **[System] [SERVICE MENU] [TESTS] [70] [x1] [EXECUTE TEST] [CONTINUE]**

In a properly working display, the following will not occur:

- complete rows or columns of stuck pixels
- more than 5 stuck pixels (not to exceed a maximum of 2 red or blue, and 3 green)
- 2 or more consecutive stuck pixels
- stuck pixels less than 6.5 mm apart

Dark Pixels Specifications

Dark "stuck on" pixels may appear against a white background. To test for these dots, press **[System] [SERVICE MENU] [TESTS] [66] [x1] [EXECUTE TEST] [CONTINUE].**

In a properly working display, the following will not occur:

- more than 12 stuck pixels (not to exceed a maximum of 7 red, green, or blue)
- more than one occurrence of 2 consecutive stuck pixels
- stuck pixels less than 6.5 mm apart

Newton's Rings

To check for the patterns known as Newton's Rings, change the display to white by pressing the following keys:

[System] [SERVICE MENU] [TESTS] [66] [x1] [EXECUTE TEST] [CONTINUE]

Figure 6-5 illustrates acceptable and non-acceptable examples of Newtons Rings.

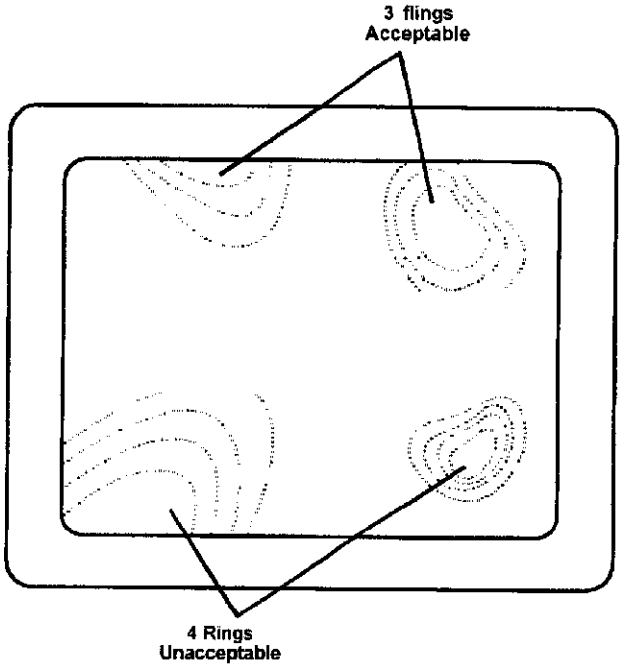


Figure 6-5. Newtons Rings

Troubleshooting a White Display

If the display is white, the A27 back light inverter is functioning properly. Connect a VGA monitor to the analyzer.

- If the image on the external monitor is normal, then suspect A2, A18, or the front panel cabling.
- If the image on the external monitor is bad, suspect the A19 GSP or cable W20 (CPU to motherboard).

Troubleshooting a Black Display

1. Remove the front panel with the exception of leaving cable W17 (A2 to motherboard) connected.
2. Press **[Preset]** while checking to see if there is a flash of light.

   If the light does not flash, suspect the front panel cabling, the display lamp, or the A27 inverter.

Troubleshooting a Display with Color Problems

1. Press **[Display] [ADJUST DISPLAY] [DEFAULT COLORS].** If this does not correct the color problems, continue with the next step.
2. Run display service test 74 as described in Chapter 10. Confirm that there are four intensities for each color.
   - If the test passes, then continue.
   - If the test fails, then suspect the front panel cabling, A2, A19, or A18.
3. Connect a VGA monitor to the analyzer.
   - If the image on the external monitor has the same color problems, then replace the A19 GSP.
   - If the image on the external monitor is acceptable, then there must be a missing color bit. Suspect the front panel cabling, A2, A19, or A18.

Front Panel Troubleshooting (A1, A2)

Check Front Panel LEDs After Preset

1. Press **[Preset]** on the analyzer.
2. Observe that all front panel LEDs turn on and, within five seconds after releasing **[Preset]**, all but the CH1 and Port 1 LED turns off. Refer to Figure 6-6.
   - If all the front panel LEDs either stay on or off, there is a control problem between A9 and A1/A2. See "Inspect Cables," located later in this chapter.
   - If, at the end of the turn on sequence, the channel 1 LED is not on and all HP-IB status LEDs are not off, continue with "Identify the Stuck Key".
   - If you suspect that one or more LEDs have burned out, replace the A1 keypad assembly.

Note Port 1 and port 2 LED problems may be caused by the malfunction of the A23 LED board or the A24 transfer switch.

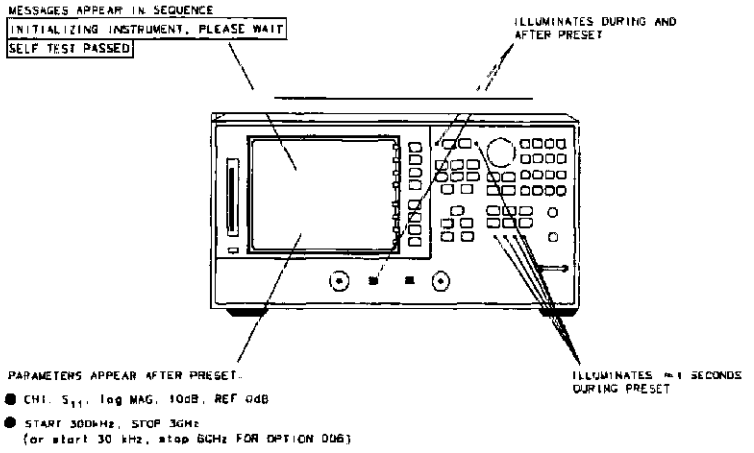


Figure 6-6. Preset Sequence

Identify the Stuck Key

Match the LED pattern with the patterns in Table 6-1. The LED pattern identifies the stuck key. Free the stuck key or replace the front panel part causing the problem.

Table 6-1. Front Panel Key Codes

Decimal Number	LED Pattern						Key	Front Panel Block
	CH1	CH2	R	L	T	S		
0							Cal	Response
1						•	3	Entry
2					•		k/m	Entry
3					•	•	Display	Response
4				•			Avg	Response
5				•		•	2	Entry
6				•	•		1	Entry
7				•	•	•	softkey 3	Softkey
8			•				softkey 5	Softkey
9			•			•	9	Entry
10			•		•		G/n	Entry
11			•		•	•	Chan 1	Active Channel
12			•	•			Chan 2	Active Channel
13			•	•		•	8	Entry
14			•	•	•		7	Entry
15			•	•	•	•	softkey 1	Softkey
16		•					Stop	Stimulus
17		•				•	Save/Recall	Instrument State
18		•			•		Seq	Instrument State
19		•			•	•	Menu	Stimulus
20		•		•			Start	Stimulus
21		•		•		•	Copy	Instrument State
22		•		•	•		System	Instrument State
23		•		•	•	•	softkey 6	Softkey
24		•	•				Scale Ref	Response
25		•	•			•	6	Entry

Table 6-1. Front Panel Key Codes (continued)

Decimal Number	LED Pattern						Key	Front Panel Block
	CH1	CH2	R	L	T	S		
26		•	•		•		M/μ	Entry
27		•	•		•	•	Meas	Response
28		•	•	•			Format	Response
29		•	•	•		•	[5]	Entry
30		•	•	•	•		[4]	Entry
31		•	•	•	•	•	[softkey] [2]	Softkey
32	•						Span	Stimulus
33	•					•	⇩	Entry
34	•				•		ENTRY OFF	Entry
35	•				•	•	Center	Stimulus
36	•			•			softkey 8	Softkey
37	•			•		•	⇧	Entry
38	•			•	•		Local	Instrument State
39	•			•	•	•	softkey 7	Softkey
40-47	Not used							
48	•	•					←	Entry
49	•	•				•	–	Entry
50	•	•			•		x1	Entry
51	•	•			•	•	Marker	Response
52	•	•		•			Marker Fctn	Response
53	•	•		•		•	.	Entry
54	•	•		•	•		0	Entry
55	•	•		•	•	•	softkey 4	Softkey

Inspect Cables

Remove the front panel assembly and visually inspect the ribbon cable that connects the front panel to the motherboard. Also, inspect the interconnecting ribbon cable between A1 and A2. Make sure the cables are properly connected. Replace any bad cables.

Test Using a Controller

If a controller is available, write a simple command to the analyzer. If the analyzer successfully executes the command, the problem is either the A2 front panel interface or W17 (A2 to motherboard ribbon cable) is faulty.

Run the Internal Diagnostic Tests

The analyzer incorporates 20 internal diagnostic tests. Most tests can be run as part of one or both major test sequences: all internal (test 0) and preset (test 1).

1. Press **[System] [SERVICE MENU] [TESTS] [0] [x1] [EXECUTE TEST]** to perform all INT tests.
2. Then press **[1] [x1]** to see the results of the preset test. If either sequence fails, press the ⇧ ⇩ keys to find the first occurrence of a FAIL message for tests 2 through 20. See Table 6-2 for further troubleshooting information.

Table 6-2. Internal Diagnostic Test with Commentary

Test	Sequence*	Probable Failed Assemblies†; Comments and Troubleshooting Hints
0 All Int	-	-: Executes tests 3-11, 13-16, 20
1 Preset	-	-: Executes tests 2-11, 14-16. Runs at power-on or preset.
2 ROM	P,AI	A9: Repeats on fail; refer to "CPU Troubleshooting (A9)" in this chapter to replace ROM or A9.
3 CMOS RAM	P,AI	A9: Replace A9.
4 Main DRAM	P,AI	A9: Repeats on fail; replace A9.
5 DSP Wr/Rd	P,AI	A9: Replace A9.
6 DSP RAM	P,AI	A9: Replace A9.
7 DSP ALU	P,AI	A9: Replace A9.
8 DSP Intrpt	P,AI	A9/A10: Remove A10, rerun test. If fail, replace A9. If pass, replace A10
9 DIF Control	P,AI	A9/A10: Most likely A9 assembly.
10 DIF Counter	P,AI	A10/A9/A12: Check analog bus node 17 for 1 MHz. If correct, A12 is verified; suspect A10.
11 DSP Control	P,AI	A10/A9: Most likely A10.
12 Fr Pan Wr/Rd	-	A2/A1/A9: Run test 23. If fail, replace A2. If pass, problem is on bus between A9 and A2 or on A9 assembly.
13 Rear Panel	AI	A16/A9: Disconnect A16, and check A9J2 pin 48 for 4 MHz clock signal. If OK, replace A16. If not, replace A9.
14 Post-reg	P,AI	A15/A8/Destination assembly: See Chapter 6, "Power Supply Troubleshooting."
15 Frac-N Cont	P,AI	A14: Replace A14.
16 Sweep Trig	P,AI	A14, A10: Most likely A14.
17 ADC Lin	-	A10: Replace A10.
18 ADC Ofs	-	A10: Replace A10.
19 ABUS Test	-	A10: Replace A10.
20 FN Count	AI	A14/A13/A10: Most likely A14 or A13, as previous tests check A10. See Chapter 7, "Source Troubleshooting."

* P= part of PRESET sequence; AI -part of ALL INTERNAL sequence

† in decreasing order of probability

If the Fault Is Intermittent

Repeat Test Function

If the failure is intermittent, do the following:

1. Press **[System] [SERVICE MENU] [TEST OPTIONS] [REPEAT ON]** to turn on the repeat function.
2. Then press **[RETURN] [TESTS].**
3 Select the test desired and press **[EXECUTE TEST].**
4. Press any key to stop the function. The test repeat function is explained in Chapter 10, "Service Key Menus and Error Messages."

HP-IB Failures

If you have performed "Step 3. Troubleshooting HP-IB Systems" in Chapter 4, "Start Troubleshooting Here," and you suspect there is an HP-IB problem in the analyzer, perform the following test It checks the internal communication path between the A9 CPU and the Al6 rear panel. It does not check the HP-IB paths external to the instrument.

Press **[System] [SERVICE MENU] [TESTS] [13] [x1] [EXECUTE TEST].**

- If the analyzer fails the test, the problem is likely to be the Al6 rear panel.
- If the analyzer passes the test, it indicates that the A9 CPU can communicate with the Al6 rear panel with a 50% confidence level. There is a good chance that the Al6 rear panel is working. This is because internal bus lines have been tested between the A9 CPU and A16, and HP-IB signal paths are not checked external to the analyzer.

7

Source Troubleshooting

Use this procedure only if you have read Chapter 4, "Start Troubleshooting Here." This chapter is divided into two troubleshooting procedures for the following problems:

- Incorrect power levels: Perform the "Power" troubleshooting checks.
- Phase lock error: Perform the "Phase Lock Error" troubleshooting checks.

The source group assemblies consist of the following:

- A3 source
- A4 sampler/mixer
- A7 pulse generator
- A11 phase lock
- A12 reference
- A13 fractional-N [analog)
- A14 fractional-N (digital)

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 8753E network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Before You Start Troubleshooting

Make sure all of the assemblies are firmly seated. Also make sure that input R has a signal of at least -35 dBm (about 0.01 Vp-p into 50 ohms) at all times to maintain phase lock.

Power

If the analyzer output power levels are incorrect but no phase lock error is present, perform the following checks in the order given:

For the following checks, make sure that the A9 switch is in the Alter position.

1. Source Default Correction Constants (Test 44)

To run this test, press **[Preset] [System] [SERVICE MENU] [TESTS] [44] [x1] [EXECUTE TEST]**. When complete, DONE should appear on the analyzer display. Use a power meter to verify that source power can be controlled and that the power level is approximately correct. If the source passes these checks, proceed with step 2. However, if FAIL appears on the analyzer display, or if the analyzer fails the checks, replace the source.

2. RF Output Power Correction Constants (Test 47)

Follow the instructions for this procedure given in Chapter 3, "Adjustments and Correction Constants." The procedure is complete when DONE appears on the analyzer display. Use a power meter to verify that power levels are now correct. If power levels are not correct, or if the analyzer fails the routine, proceed with step 3.

3. Sampler Magnitude and Phase Correction Constants (Test 53)

Follow the instructions for this procedure given in Chapter 3, "Adjustments and Correction Constants." The procedure is complete when DONE appears on the analyzer display. Next, repeat step 2. If the analyzer fails the routine in step 2, replace the source.

If the analyzer fails the routine in step 3, replace the source.

Phase Lock Error

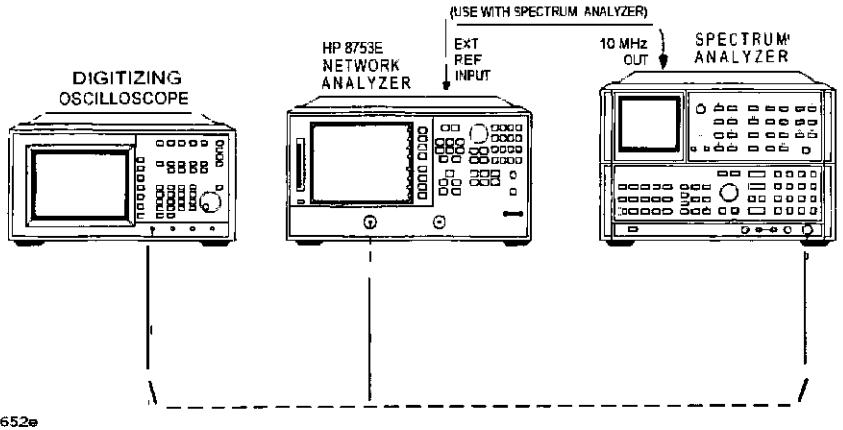


Figure 7-1. Basic Phase Lock Error Troubleshooting Equipment Setup

Troubleshooting tools include the assembly location diagram and phase lock diagnostic tools. The assembly location diagram is on the underside of the instrument top cover. The diagram shows major assembly locations and RF cable connections. The phase lock diagnostic tools are explained in the "Source Group Troubleshooting Appendix" and should be used to troubleshoot phase lock problems. The equipment setup shown in Figure 7-l can be used throughout this chapter.

Phase Lock Loop Error Message Check

Phase lock error messages may appear as a result of incorrect pretune correction constants To check this possibility, perform the pretune correction constants routine.

The four phase lock error messages, listed below, are described in the "Source Group Troubleshooting Appendix" at the end of this chapter.

- NO IF FOUND: CHECK R INPUT LEVEL
- NO PHASE LOCK: CHECK R INPUT LEVEL
- PHASE LOCK CAL FAILED

- PHASE LOCK LOST

1. Make sure the A9 CC Jumper is in the ALTER position:
   a. Remove the power line cord from the analyzer.
   b. Set the analyzer on its side.
   c. Remove the two corner bumpers from the bottom of the instrument with a T-15 TORX screwdriver.
   d. Loosen the captive screw on the bottom cover's back edge.
   e. Slide the cover toward the rear of the instrument.
   f. Move the jumper to the ALT position as shown in Figure 7-2.
   g. Replace the bottom cover, corner bumpers, and power cord.

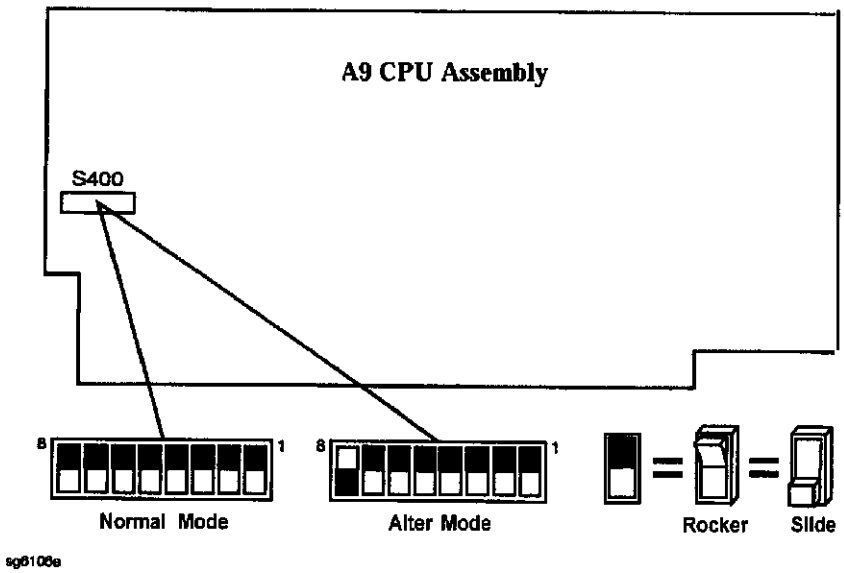


Figure 7-2. Jumper Positions on the A9 CPU

2. Switch on the analyzer and press **[System] [SERVICE MENU] [TESTS] [46] [x1] [EXECUTE TEST]** to generate new analog bus correction constants. Then press **[System] [SERVICE MENU] [TESTS] [45] [x1] [EXECUTE TEST]** to generate default pretune correction constants.

   Press **[System] [SERVICE MENU] [TESTS] [48] [x1] [EXECUTE TEST] [YES]** to generate new pretune correction constants.

3. Press **[Preset]** and observe the analyzer display:

   a. No error message: restore the A9 CC jumper to the NRM position. Then refer to "Post-Repair Procedures" in Chapter 14 to verify operation.

   b. Error message visible: continue with "A4 Sampler/Mixer Check".

A4 Sampler/Mixer Check

The A4, A5, and A6 (R, A and B) sampler/mixers are similar in operation. Any sampler can be used to phase lock the source. To eliminate the possibility of a faulty R sampler, follow this procedure.

1. Remove the W8 cable (A11J1 to A4) from the R-channel sampler (A4) and connect it to either the A-channel sampler (A5) or the B-channel sampler (A6). Refer to Figure 7-3.

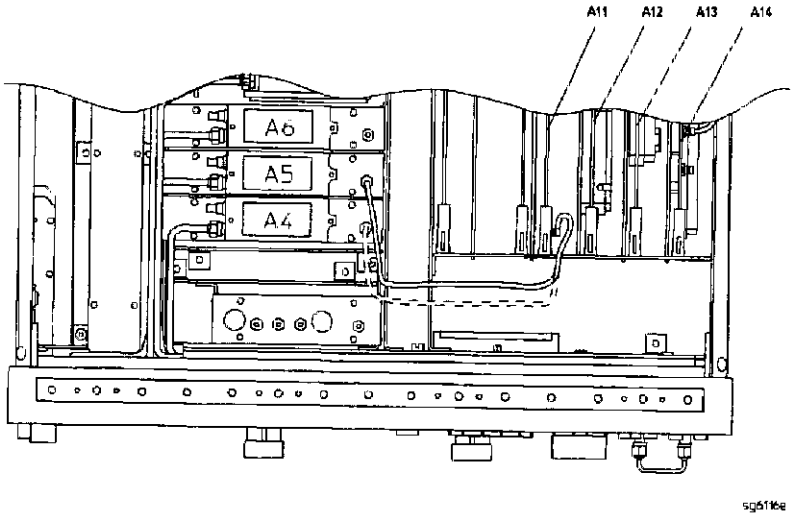


Figure 7-3. Sampler/Mixer to Phase Lock Cable Connection Diagram

2. If you connected W8 to:

   - **A5**, press **[Meas] [Refl FWD: S11 (A/R)]**

   - **A6**, press **[Meas] [Ref 1 REV: S22 (B/R)]**

3. Ignore the displayed trace, but check for phase lock error messages. If the phase lock problem persists, the R-channel sampler is **not** the problem.

A3 Source and All Phase Lock Check

This procedure checks the source and part of the phase lock assembly. It opens the phase-locked loop and exercises the source by varying the source output frequency with the A11 pretune DAC.

Note If the analyzer failed internal test 48, default pretune correction constants were stored which may result in a constant offset of several MHz. Regardless, continue with this procedure.

Note Use a spectrum analyzer for problems above 100 MHz.

1. Connect the oscilloscope or spectrum analyzer as shown in Figure 7-1. (Set the oscilloscope input impedance to 50 ohms.)
2. Press **[Preset] [System] [SERVICE MENU] [SERVICE MODES] [SRC ADJUST MENU] [SRC TUNE ON] [SRC TUNE FREQ]** to activate the source tune (SRC TUNE) service mode.
3. Use the front panel knob or front panel keys to set the pretune frequency to 300 kHz, 30 MHz, and 40 MHz. Verify the signal frequency on the oscilloscope.

Note In SRC TUNE mode, the source output frequency changes in 1 to 2 MHz increments and should be 1 to 6 MHz above the indicated output frequency.

4. Check for the frequencies indicated by Table 7-1.

Table 7-1. Output Frequency in SRC Tune Mode

Setting	Observed Frequency
300 kHz	1.3 to 6.3 MHz
30 MHz	31 to 36 MHz
40 MHz	41 to 46 MHz

5. The signal observed on an oscilloscope should be as solid as the signal in Figure 7-4.

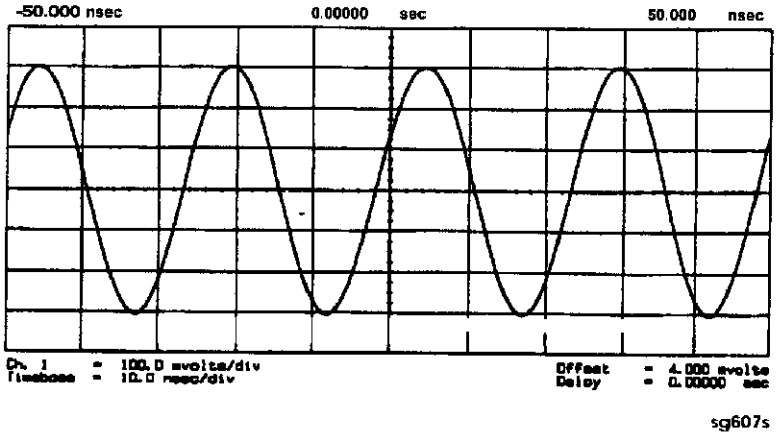


Figure 7-4. Waveform Integrity in SRC Tune Mode

6. The signal observed on the spectrum analyzer will appear jittery as in Figure 7-5 (B), not solid as in Figure 7-5 (A). This is because in SRC TUNE mode the output is not phase locked.

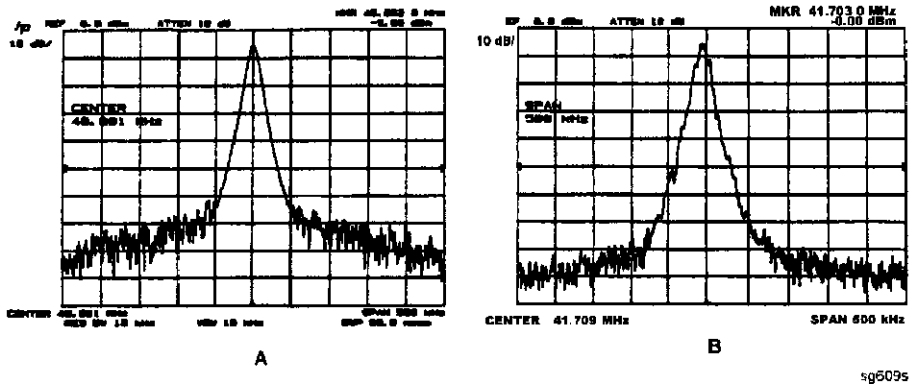


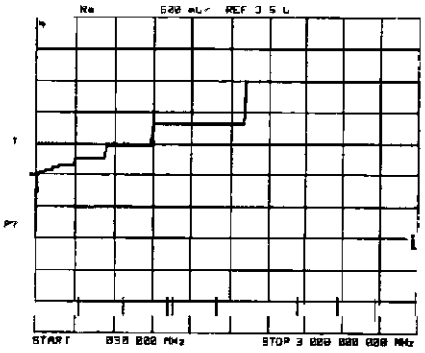
Figure 7-5.
Phase Locked Output Compared to Open Loop Output in SRC Tune Mode

7. Press **[Menu] [POWER]** to vary the power and check for corresponding level changes on the test instrument. (A power change of 20 dB will change the voltage observed on the oscilloscope by a factor of ten.)
8. Note the results of the frequency and power changes:
   - If the frequency and power output changes are correct, skip ahead to "A12 Reference Check" located in this chapter.
   - If the frequency changes are not correct, continue with "YO Coil Drive Check with Analog Bus".
   - If the power output changes are not correct, check analog bus node 3.
     a. Press **[System] [SERVICE MENU] [ANALOG BUS ON] [Meas] [ANALOG IN Aux Input] [Format] [MORE] [REAL] [3] [x1].**
     b. Press **[Marker] [2] [G/n].** The marker should read approximately 434 mU.
     c. Press **[Marker] [4] [G/n].** The marker should read approximately 646 mU.

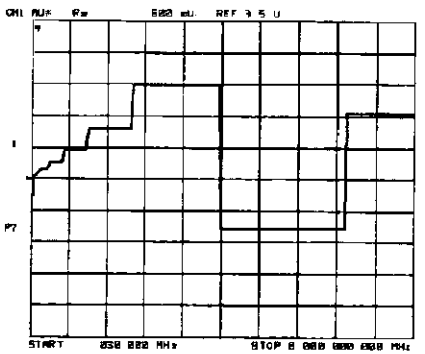
YO Coil Drive Check with Analog Bus

Note If the analog bus is not functional, perform the "YO Drive Coil Check with Oscilloscope" test.

1. Press **[Preset] [System] [SERVICE MENU] [ANALOG BUS ON] [SERVICE MODES] [SOURCE PLL OFF] [Meas] [ANALOG IN Aux Input].**
2. Then press **[16] [x1] [Format [MORE] [REAL] [Scale Ref] [AUTOSCALE].** This keystroke sequence lets you check the pretune DAC and the All output to the YO coil drive by monitoring the 1 V/GHz signal at analog bus node 16,
3. Compare the waveform to Figure 7-6 If the waveform is incorrect, the A11 phase lock assembly is faulty.



3 GHz 8753D



8 GHz 8753D

sg629s

Figure 7-6. 1 V/GHz at Analog Bus Node 16 with Source PLL Off.

YO Coil Drive Check with Oscilloscope

Note Use the large extender board for easy access to the voltage points. The extender board is included with the HP 8753 Tool Kit. See Chapter 13, "Replaceable Parts", for part numbers and ordering information.

1. Connect oscilloscope probes to A11P1-1 and A11P1-2. The YO coil drive signal is actually two signals whose voltage difference drives the coil.
2. Press **[Preset] [System] [SERVICE MENU] [SERVICE MODES] [SOURCE PLL OFF]** to operate the analyzer in a swept open loop mode.
3. Monitor the two YO coil drive lines. In source tune mode the voltage difference should vary from approximately 3.5 to 5.0 volts as shown in Figure 7-7
   - If the voltages are not correct, replace the faulty A11 assembly.
   - If the output signals from the A11 assembly are correct, replace the faulty A3 source assembly.
   - If neither the A11, nor the A3 assembly is faulty, continue with the next check.

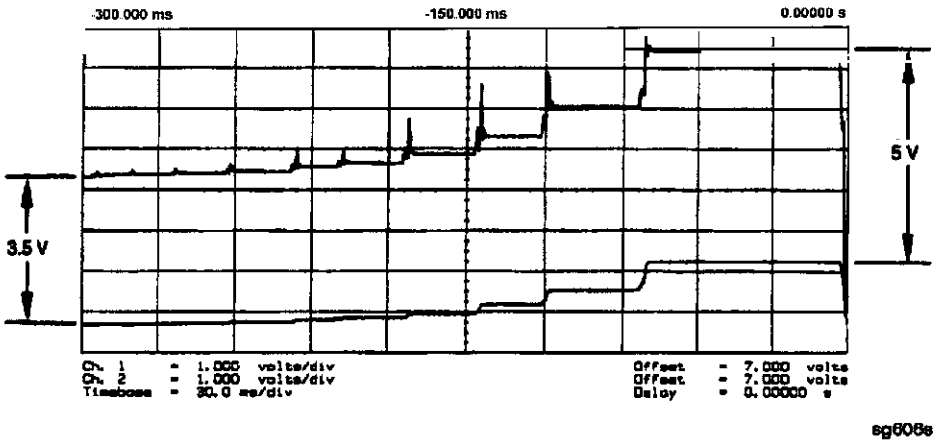


Figure 7-7.
YO- and YO+ Coil Drive Voltage Differences with SOURCE PLL OFF

A12 Reference Check

The signals are evaluated with pass/fail checks. The most efficient way to check the A12 frequency reference signals is to use the analog bus while referring to Table 7-2.

Alternatively, you can use an oscilloscope, while referring to Table 7-3 and Figure 7-8 through Figure 7-14. If any of the observed signals differs from the figures, there is a 90% probability that the A12 assembly is faulty. Either consider the A12 assembly defective or perform the "A12 Digital Control Signals Check".

Both of these procedures are described ahead.

Analog Bus Method

1. Press **[Preset] [System] [SERVICE MENU] [ANALOG BUS ON] [Meas] [ANALOG IN Aux Input] [ANALOG BUS]** to switch on the analog bus and its counter.
2. Press **[21] [x1]** to count the frequency of the 100 kHz signal.
3. Press **[Menu] [CW FREQ] [500] [k/m].** Verify that the counter reading (displayed on the analyzer next to cnt :) matches the corresponding 100 kHz value for the CW frequency. (Refer to Table 7-2.)
4. Verify the remaining CW frequencies, comparing the counter reading with the value in Table 7-2:
   - Press **[2] [M/μ].**
   - Press **[50] [M/μ].**

Table 7-2. Analog Bus Check of Reference Frequencies

CW Frequency	Analog Bus Node 21 100 kHz	Analog Bus Node 24 2nd LO	Analog Bus Node 25 FLREF
500 kHz	0.100 MHz	0.604 MHz	0.500 MHz
2 MHz	0.100 MHz	2.007 MHz	2.000 MHz
50 MHz	0.100 MHz	0.996 MHz	1.000 MHz

NOTE: The counter should indicate the frequencies listed in this table to within ±0.1%. Accuracy may vary with gate time and signal strength.

5. Press **[24] [x1]** to count the frequency of the 2nd LO signal.
6. Press **[Menu] [CW FREQ] [500] [k/m]**. Verify that the counter reading matches the corresponding 2nd LO value for the CW frequency. (Refer to Table 7-2.)
7. Verify the remaining CW frequencies, comparing the counter reading with the value in Table 7-2:
   - Press **[2] [M/μ]**
   - Press **[50] [M/μ]**
8. Press **[25] [x1]** to count the frequency of the PLREF signal.
9. Press **[Menu] [CW FREQ] [500] [k/m]**. Verify that the counter reading matches the corresponding PLREF value for the CW frequency. (Refer to Table 7-2.)
10. Verify the remaining CW frequencies, comparing the counter reading with the value in Table 7-2:
    - Press **[2] [M/μ].**
    - Press **[50] [M/μ].**
11. Check the results.
    - If all the counter readings match the frequencies listed in Table 7-2, skip ahead to "A13/A14 Fractional-N Check".
    - If the counter readings are incorrect at the 500 kHz and 2 MHz settings only, go to "FN LO at A12 Check".
    - If all the counter readings are incorrect at all three CW frequencies, the counter may be faulty. Perform the "Oscilloscope Method" check of the signals described below. (If the signals are good, either the A10 or A14 assemblies could be faulty.)

Oscilloscope Method

You need not use the oscilloscope method unless the analog bus is non-functional or any of the signals fail the specifications listed in Table 7-2.

If the analog bus is non-functional or the previous check has revealed questionable signals, observe the signal(s) with an oscilloscope. Table 7-3 identifies a convenient test point and a plot for the five signals listed.

Table 7-3. A12 Reference Frequencies

Mnemonic	Signal Description	Location	See Figure	Analyzer Setting
FN 100kHzREF	100 kHz Reference	A13TP5	Figure 7-8	any
REF	Phase Lock Reference	A11TP9	Figure 7-9	≥16 MHz CW
REF	Phase Lock Reference	A11TP9	Figure 7-10	5 MHz CW
FN LO*	Fractional-N LO	A14J2	Figure 7-11	10 MHz CW
4MHz REF	4 MHz Reference	A12TP9	Figure 7-12	any
2ND LO+/-	Second LO	A12P1-2,4	Figure 7-13	≥16 MHz CW
2ND LO+/-	Second LO	A12P1-2,4	Figure 7-14	14 MHz CW

* Not an A12 signal, but required for A12 lowband operation.

100 kHz Pulses

The 100 kHz pulses are very narrow and typically 1.5 V in amplitude. You may have to increase the oscilloscope intensity to see these pulses. (See Figure 7-8.)

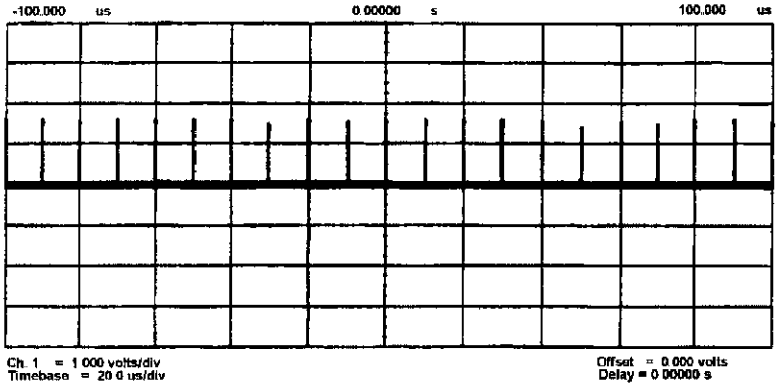


Figure 7-8. Sharp 100 kHz Pulses at A13TP5 (any frequency)

PLREF Waveforms

REF Signal At A11TP9. REF is the buifered PLREF+ signal The 1st IF is phase locked to this signal. Use an oscilloscope to observe the signal at the frequencies noted in Figure 7-9 and Figure 7-10.

High Band REF Signal. In high band the REF signal is a constant 1 MHz square wave as indicated by Figure 7-9.

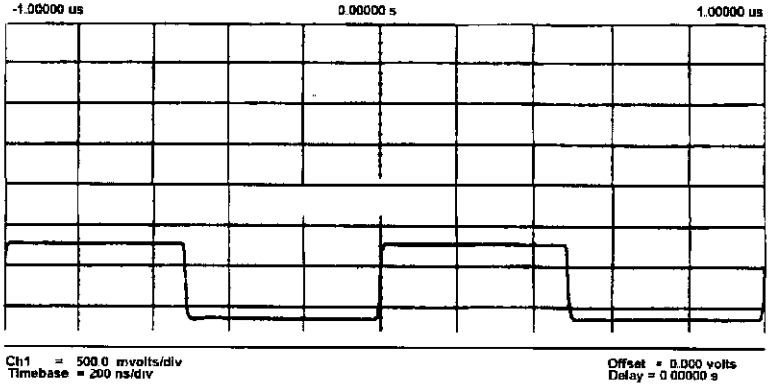


Figure 7-9. High Band REF Signal (≥16 MHz CW)

Low Band REF Signal. In low band this signal follows the frequency of the RF output signal. Figure 7-10 illustrates a 5 MHz CW signal.

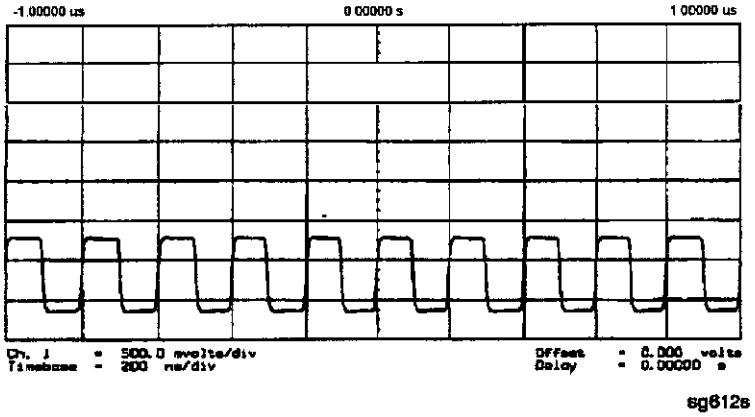


Figure 7-10. REF Signal at A11TP9 (5 MHz CW)

- If REF looks good, skip ahead to "4 MHz Reference Signal".
- If REF is bad in low band, continue with "FN LO at A12 Check".

FN LO at A12 Check

1. Use an oscilloscope to observe the FN LO from A14 at the cable end of A14J2. Press **[Preset] [System] [SERVICE MENU] [SERVICE MODES] [FRACN TUNE ON]** to switch on the fractional-N service mode.
2. Use the front panel knob to vary the frequency from 30 to 60 MHz. The signal should appear similar to Figure 7-11. The display will indicate 10 to 60.8 MHz.
   - If the FN LO signal is good, the A12 assembly is faulty.
   - If the FN LO signal is not good, skip ahead to "A13/A14 Fractional-N Check".

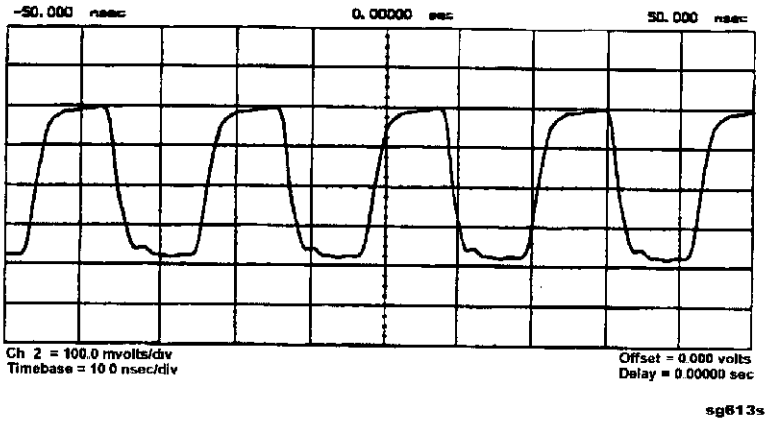
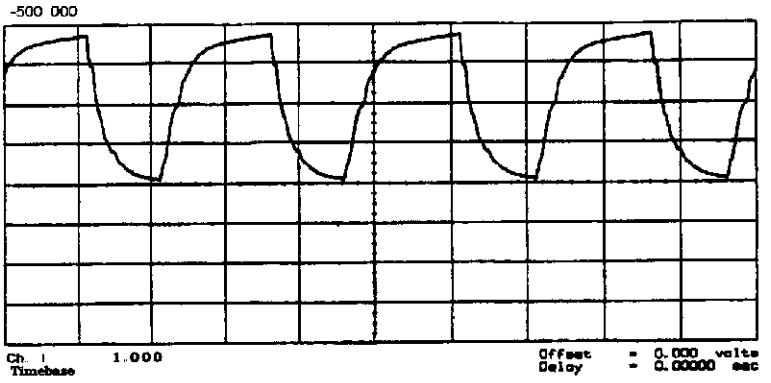


Figure 7-11. Typical FN LO Waveform at A12J1

4 MHz Reference Signal

This reference signal is used to control the receiver. If faulty, this signal can cause apparent source problems because the CPU uses receiver data to control the source. At A12TP9 it should appear similar to Figure 7-12.



sg61 4s

Figure 7-12. 4 MHz Reference Signal at A12TP9 (Preset)

2ND LO Waveforms

The 2nd LO signals appear different in phase and shape at different frequencies.

90 Degree Phase Offset of 2nd LO Signals in High Band. In high band, the 2nd LO is 996 kHz. As indicated by Figure 7-13, the 2nd LO actually consists of two signals 90 degrees out of phase.

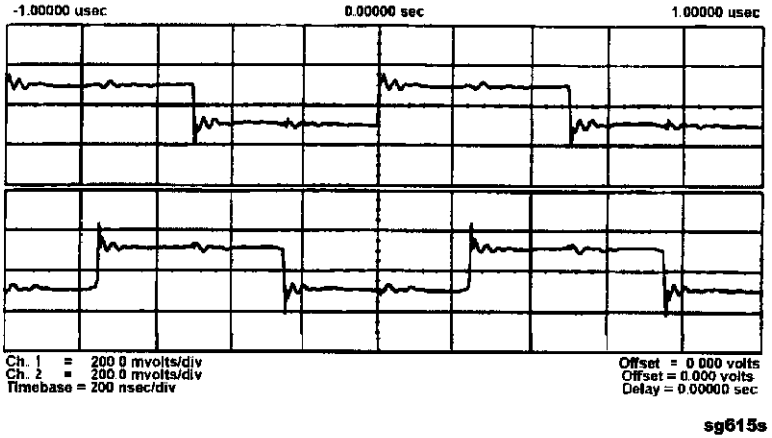


Figure 7-13.
90 Degree Phase Offset of High Band 2nd LO Signals (≥16 MHz CW)

In-Phase 2nd LO Signals in Low Band. The 2nd LO signals in low band, as shown in Figure 7-14, are not phase shifted. In low band these signals track the RF output with a 4 kHz offset.

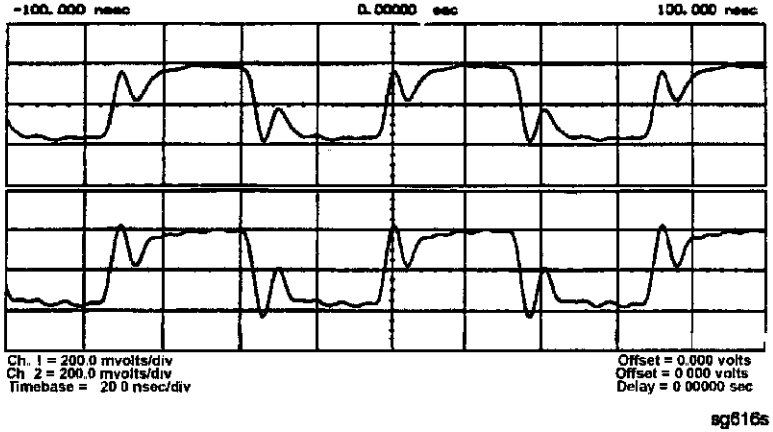


Figure 7-14. In-Phase Low Band 2nd LO Signals (14 MHz CW)

If any of the signals of Table 7-2 are incorrect, the probability is 90% that the A12 assembly is faulty. Either consider the A12 assembly faulty or perform the "A12 Digital Control Signals Check" described ahead.

A12 Digital Control Signals Check

Several digital control signals must be functional for the A12 assembly to operate properly. Check the control lines listed in Table 7-4 with the oscilloscope in the high input impedance setting.

Table 7-4. A12-Related Digital Control Signals

Mnemonic	Signal Description	Location	See Figure	Analyzer Setting
L ENREF	L-Reference Enable	A12P2-6	Figure 7-15	Preset
L HB	L-High Band	A12P2-32	Figure 7-16	Preset
L LB	L-Low Band	A12P1-23	Figure 7-16	Preset

L ENREF Line. This is a TTL signal. To observe it, trigger on the negative edge. In preset state, the signal should show activity similar to Figure 7-15.

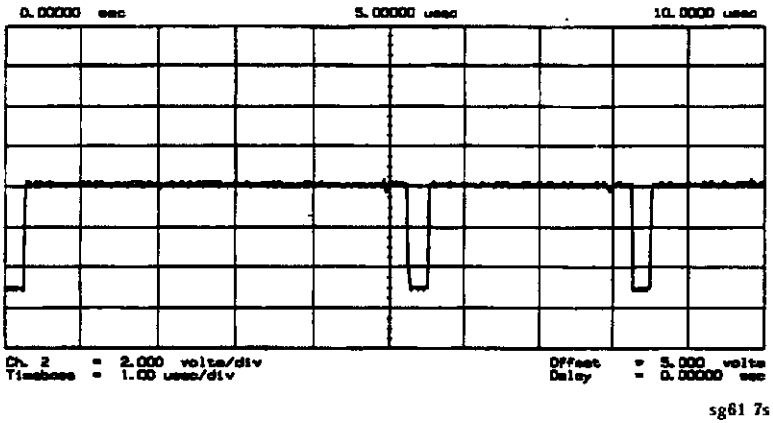


Figure 7-15. L ENREF Line at 12P2-16 (Preset)

L HB and L LB Lines. These complementary signals toggle when the instrument switches from low band to high band as illustrated by Figure 7-16.

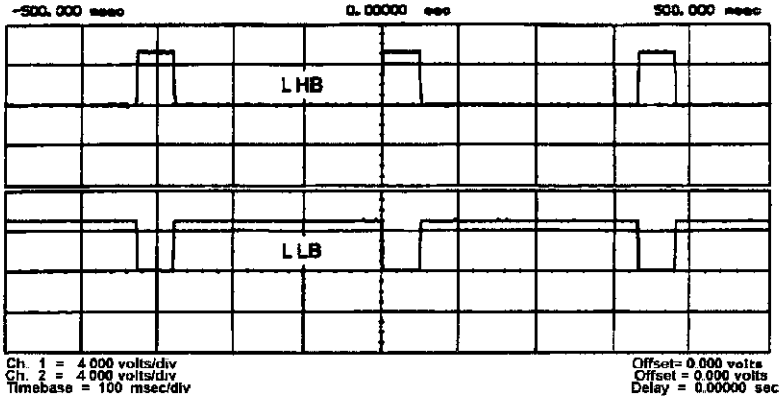


Figure 7-16. Complementary L HB and L LB Signals (Preset)

If all of the digital signals appeared good, the A12 assembly is faulty.

A13/A14 Fractional-N Check

Use the analog bus or an oscilloscope to check the A14 VCO's ability to sweep from 30 MHz to 60 MHz. The faster analog bus method should suffice unless problems are detected.

Fractional-N Check with Analog Bus

1. Press **[Preset] [System] [SERVICE MENU] [ANALOG BUS ON] [Meas] [ANALOG IN Aux Input] [FRAC N]** to switch on the analog bus and the fractional-N counter.
2. Then press **[Menu] [CW FREQ]** to set the analyzer to CW mode.
3. Set the instrument as indicated in Table 7-5 and see whether the VCO generates the frequencies listed.

Table 7-5. VCO Range Check Frequencies

Instrument Setting	Counter Reading
31 MHz	30±0.030 MHz
60.999999 MHz	60±0.060 MHz

4. Check the counter reading at the frequencies indicated.
   - If the readings are within the limits specified, the probability is greater than 90% that the fractional-N assemblies are functional. Either skip ahead to the "A7 Pulse Generator Check" or perform the more conclusive "A14 VCO Range Check with Oscilloscope" described below.
   - If the readings fail the specified limits, perform the "A14 VCO Exercise".

A14 VCO Range Check with Oscilloscope

1. Remove the W9 HI OUT cable (A14J1 to A7) from the A7 assembly and connect it to an oscilloscope set for 50 ohm input impedance Switch on the analyzer.
2. Press **[Preset] [System] [SERVICE MENU] [SERVICE MODES] [FRACN TUNE ON]** to activate the FRACN TUNE service mode. See Chapter 10, "Service Key Menus and Error Messages", for more information on the FRACN TUNE mode.
3. Vary the fractional-N VCO frequency with the front panel knob and check the signal with the oscilloscope. The waveform should resemble Figure 7-17, Figure 7-18, and Figure 7-19.

   If the fractional-N output signals are correct, continue source troubleshooting by skipping ahead to "A7 Pulse Generator Check".

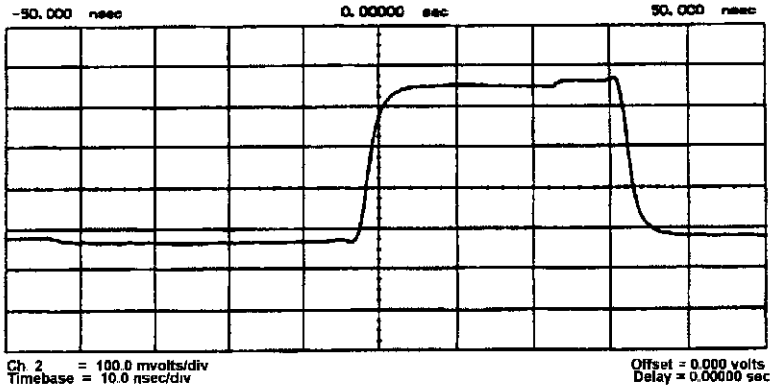


Figure 7-17. 10 MHz HI OUT Waveform from A14J1

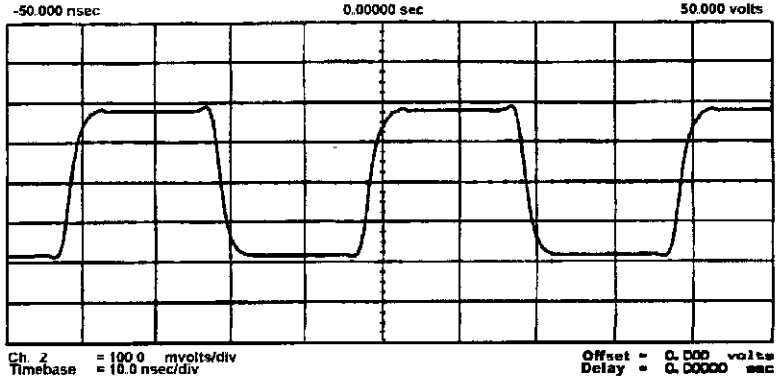


Figure 7-18. 25 MHz HI OUT Waveform from A14J1

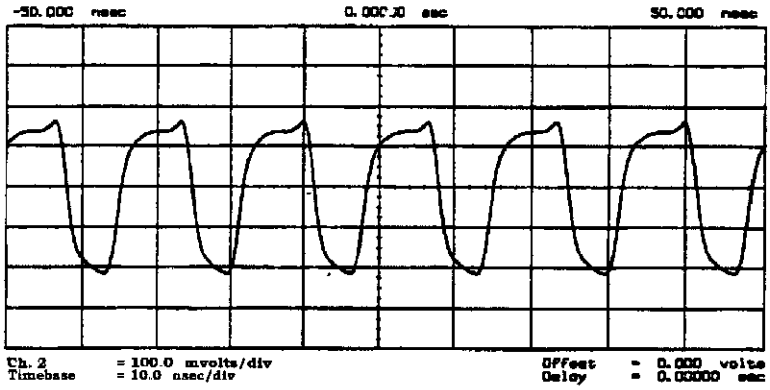


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Figure 7-19. 60 MHz HI OUT Waveform from A14J1

A14 VCO Exercise

The nominal tuning voltage range of the VCO is +10 to -5 volts. When the analyzer is in operation, this voltage is supplied by the A13 assembly. This procedure substitutes a power supply for the A13 assembly to check the frequency range of the A14 VCO.

1. Switch off the analyzer and remove the A13 assembly.
2. Put the A14 assembly on an extender board and switch on the instrument.
3. Prepare to monitor the VCO frequency, either by:
   a. Activating the analog bus and setting the internal counter to the FRACN node, or
   b. Connecting an oscilloscope to A14J2 (labeled LO OUT) and looking for waveforms similar to Figure 7-20.

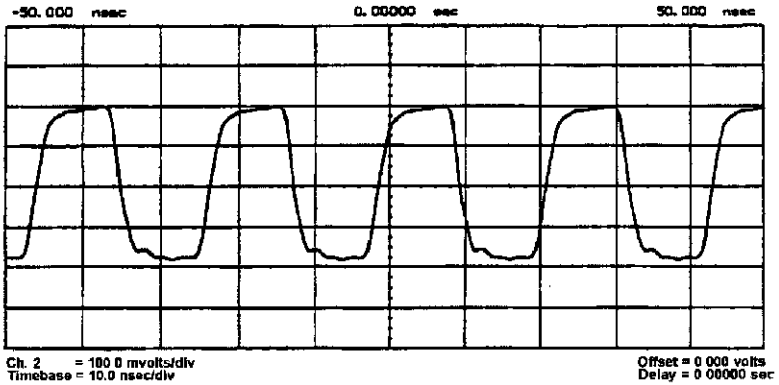

Figure 7-20. LO OUT Waveform at A14J2

4. Vary the voltage at A14TP14 from +10 to -5 volts either by:
   a. Connecting an appropriate external power supply to A14TP14, or
   b. First jumping the +15 V internal power supply from A8TP8 to A14TP14 and then jumping the -5.2 V supply from A8TP10 to A14TP14.
5. Confirm that the VCO frequency changes from approximately 30 MHz or less to 60 MHz or more.
6. If this procedure produces unexpected results, the A14 assembly is faulty.
7. If this procedure produces the expected results, continue with the "A14 Divide-by-N Circuit Check".

A14 Divide-by-N Circuit Check

Note The A13 assembly should still be out of the instrument and the A14 assembly on an extender board.

1. Ground A14TP14 and confirm (as in the A14 VCO Exercise) that the VCO oscillates at approximately 50 to 55 MHz.
2. Put the analyzer in CW mode (to avoid relock transitions) and activate the FRACN TUNE service mode.
3. Connect an oscilloscope to A14J3 and observe the output.
4. With the FRACN TUNE service feature, vary the frequency from 30 MHz to 60.8 MHz.
5. The period of the observed signal should vary from 5.5 µs to 11 µs
   - If this procedure produces unexpected results, the A14 assembly is faulty.
   - If this procedure produces the expected results, perform the "A14-to-A13 Digital Control Signals Check.".
6. Remember to replace the A13 assembly.

A14-to-A13 Digital Control Signals Check.

The A14 assembly generates a TTL cycle start (CST) signal every 10 microseconds. If the VCO is oscillating and the CST signal is not detectable at A14TP3, the A14 assembly is non-functional.

Use the CST signal as an external trigger for the oscilloscope and monitor the signals in Table 7-6. Since these TTL signals are generated by A14 to control A13, check them at A13 first. Place A13 on the large extender board. The signals should look similar to Figure 7-21. If these signals are good, the A13 assembly is defective.

Table 7-6. A14-to-A13 Digital Control Signal Locations

Mnemonic	A13 Location	A14 Location
CST	none	TP3
L FNHOLD	P2-2	P2-2
FNBIAS	P2-5	P2-5
API1	P2-32	P2-32
API2	P2-3	P2-3
API3	P2-34	P2-34
API4	P2-4	P2-4
API5	P2-35	P2-35
NLATCH	P1-28	P1-58

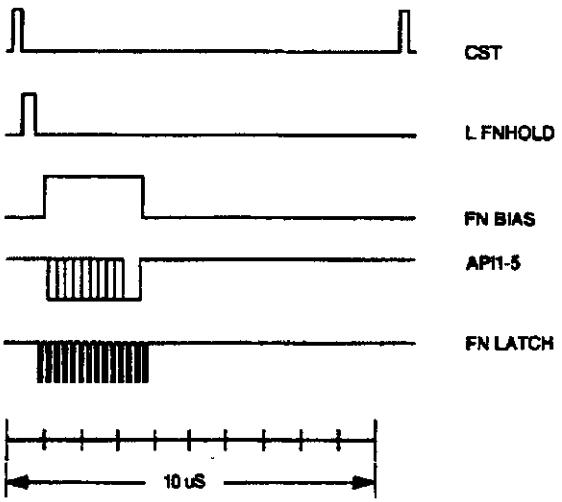

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Figure 7-21. A14 Generated Digital Control Signals

H MB Line. This signal is active during the 16 MHz to 31 MHz sweep. The upper trace of Figure 7-22 shows relative inactivity of this signal during preset condition The lower trace shows its status during a 16 MHz to 31 MHz sweep with inactivity during retrace only.

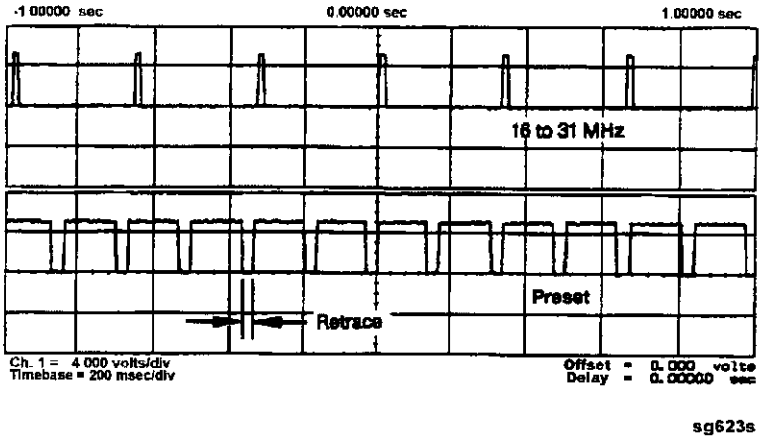

Figure 7-22.
H MB Signal at A14P1-5 (Preset and 16 MHz to 31 MHz Sweep)

A7 Pulse Generator Check

The pulse generator affects phase lock in high band only. It can be checked with either a spectrum analyzer or an oscilloscope.

A7 Pulse Generator Check with Spectrum Analyzer

1. Remove the A7- to-A6 SMB cable (W7) from the A7 pulse generator assembly. Set the analyzer to generate a 16 MHz CW signal. Connect the spectrum analyzer to the A7 output connector and observe the signal. The A7 comb should resemble the spectral display in Figure 7-23.

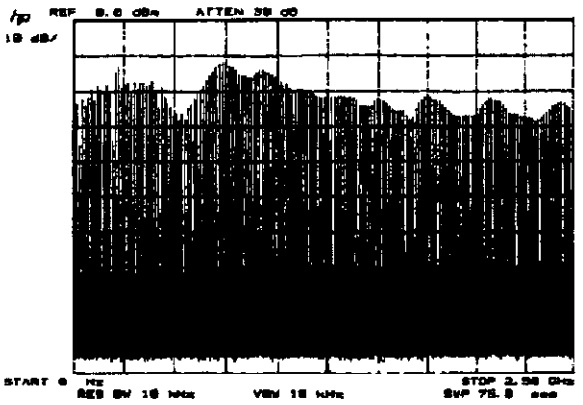

Figure 7-23. Pulse Generator Output

2. If the analyzer malfunction relates to a particular frequency or range, look more closely at the comb tooth there. Adjust the spectrum analyzer span and bandwidth as required. Even at 3 GHz, the comb should look as clean as Figure 7-24. For Option 006 instruments at 6 GHz, the comb tooth level should be approximately -46 dBm.

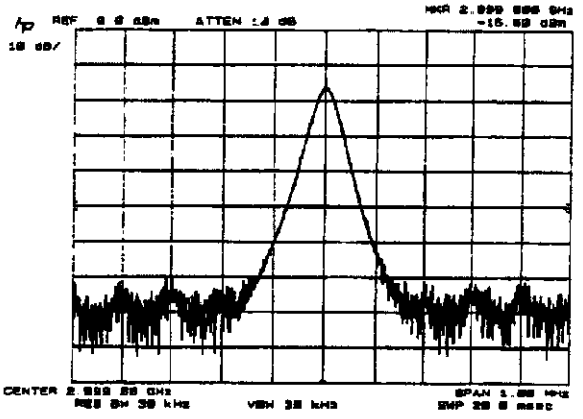

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Figure 7-24. High Quality Comb Tooth at 3 GHz

3. If the signal at the A7 output is good, check the A7-to-A4 cable
4. If the signal is not as clean as Figure 7-24, observe the HI OUT input signal to the A7 assembly.
   a. On the network analyzer, press **[System] [SERVICE MENU] [SERVICE MODES] [PLL AUTO OFF]**. Otherwise do not readjust the instrument. Remove the A14-to-A7 SMB cable (W9) from the A7 pulse generator assembly (CW ≈ 16 MHz).
   b. Set the spectrum analyzer to a center frequency of 45 MHz and a span of 30 MHz. Connect it to the A14-to-A7 cable still attached to the A14 assembly. Narrow the span and bandwidth to observe the signal closely.
5. If the HI OUT signal is as clean as Figure 7-25, the A7 assembly is faulty.

   Otherwise, check the A14-to-A7 cable or recheck the A13/A14 fractional-N as described ahead.

Rechecking the A13/A14 Fractional-N

Some phase lock problems may result from phase noise problems in the fractional-N loop. Ib troubleshoot this unusual failure mode, do the following.

1. Set the network analyzer at 60 MHz in the FRACN TUNE mode.

2. Use a spectrum analyzer, to examine the HI OUT signal from the A14 assembly. The signal should appear as clean as Figure 7-25. The comb shape may vary from pulse generator to pulse generator

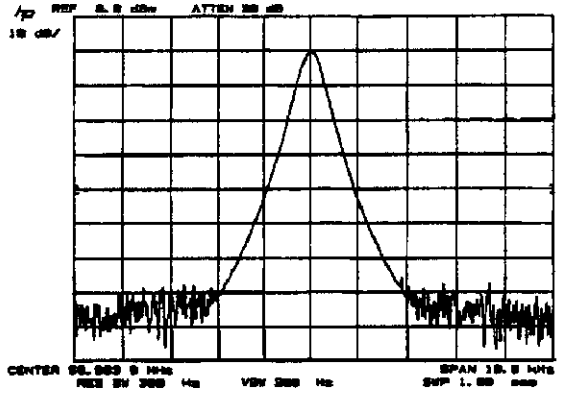

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Figure 7-25. Stable HI OUT Signal in FRACN TUNE Mode

A7 Pulse Generator Check with Oscilloscope

Perform this check if a spectrum analyzer is not available.

1. Remove the A4-to-A11 SMB cable from the A4 (R) sampler/mixer output Connect the oscilloscope to the A4 output (1st IF).
2. Activate the FRACN TUNE service mode and tune the fractional-N to 50 MHz. Press **[System] [SERVICE MENU] [SERVICE MODES] [FRACN TUNE ON] [50]** [M/μ]
3. Activate the SRC TUNE service mode of the analyzer and tune the source to 50 MHz. Press **[SRC TUNE ON] [SRC TUNE FREQ] [50] [M/μ]**
4. Set the SRC TUNE frequency to those listed in Table 7-7 and observe the 1st IF waveforms. They should appear similar to Figure 7-26.
   - If the signals observed are proper, continue with "A11 Phase Lock Check".
   - If the signals observed are questionable, use a spectrum analyzer to perform the preceding "A7 Pulse Generator Check with Spectrum Analyzer".

Table 7-7. 1st IF Waveform Settings

SRC TUNE	FRACN	Harmonic	1st IF
50 MHz	50 MHz	1	1 to 6 MHz
250 MHz	50 MHz	5	1 to 6 MHz
2550 MHz	50 MHz	51	1 to 6 MHz

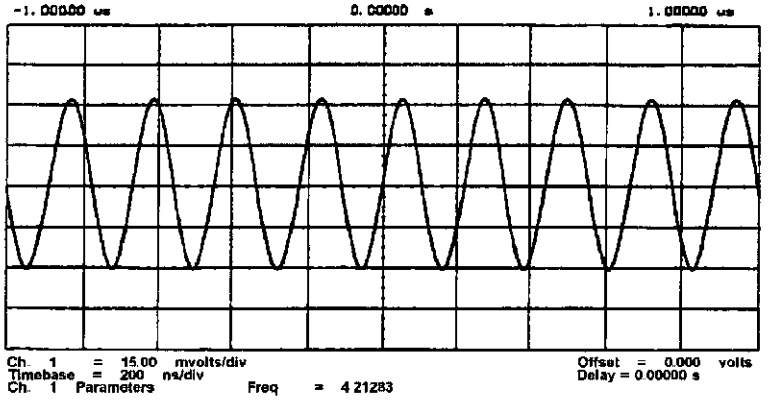


Figure 7-26. Typical 1st IF Waveform in FRACN TUNE/SRC TUNE Mode

A11 Phase Lock Check

At this point, the A11 phase lock assembly appears to be faulty (its inputs should have been verified already). Nevertheless, you may elect to use the phase lock diagnostic routines or check the relevant signals at the assembly itself for confirmation.

Note If external source mode is the only operating mode with phase lock problems, replace the A11 phase lock assembly.

Phase Lock Check with PLL DIAG

Refer to "Phase Lock Diagnostic Tools" in "Source Group Troubleshooting Appendix" at the end of this chapter for an explanation of the error messages and the diagnostic routines. Follow the steps there to determine in which state the phase lock is lost.

- If **NO IF FOUND** is displayed, confirm that the analog bus is functional and perform the "Source Pretune Correction Constants (Test 48)" as outlined in Chapter 3, "Adjustments and Correction Constants."
- If phase lock is lost in the ACQUIRE state, the A11 assembly is faulty.
- If phase lock is lost in the TRACK state, troubleshoot source phase lock loop components other than the A11 assembly.

Phase Lock Check by Signal Examination

To confirm that the A11 assembly is receiving the signals required for its proper operation, perform the following steps.

1. Place the A11 assembly on the large extender board.
2. Switch on the analyzer and press **[Preset]**
3. Check for the signals listed in Table 7-8.

Table 7-8. A11 Input Signals

Mnemonic	I/O	Access	see Figure	Notes
FM COIL –	O	A11P1-3,33	Figure 7-27	Aids YO COIL in setting YIG. Press [Preset] [Menu] [NUMBER OF POINTS] [3] [x1] to observe this signal.
REF	I	A11TP9	Figure 7-9, Figure 7-10	Observe both low band and high band CW frequencies.
YO COIL +	O	A11P1-2,32	Figure 7-7	Use [SOURCE PLL OFF]
YO COIL -	O	A11P1-1,31	Figure 7-7	
1ST IF	I	A11 PL IF IN	Figure 7-26	Check for 1 MHz with tee a A11 jack (not at cable end) in high band.

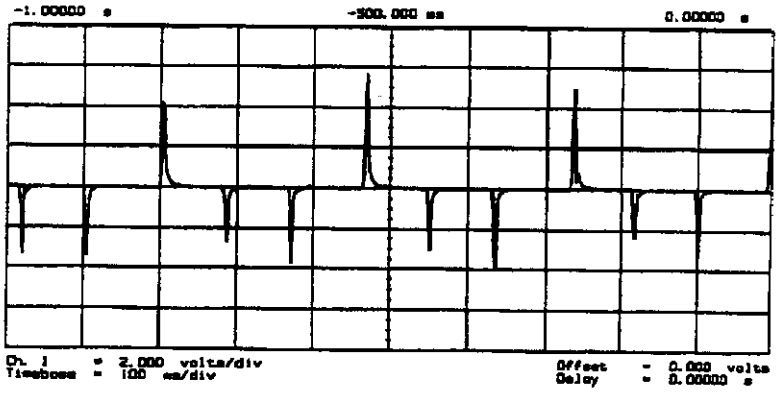


Figure 7-27. FM Coil - Plot with 3 Point Sweep

4. If any of the input signal is not proper, refer to the overall block diagram in Chapter 4, "Start Troubleshooting Here, " as an aid to trouble shooting the problem to its source.
5. If any of the output signals is not proper, the A11 assembly is faulty.

Source Group Troubleshooting Appendix

Troubleshooting Source Problems with the Analog Bus

The analog bus can perform a variety of fast checks. However, it too is subject to failure and thus should be tested prior to use. You should have done this in Chapter 4, "Start Troubleshooting Here."

To use the analog bus to check any one of the nodes, press **[Preset] [System] [SERVICE MENU] [ANALOG BUS In].** Then press **[Meas] [ANALOG IN Aux Input]** and enter the analog bus node number followed by **[x1].** Refer to "Analog Bus" in Chapter 10, "Service Key Menus and Error Messages", for additional information.

Phase Lock Diagnostic Tools

- error messages

- diagnostic routines

Phase Lock Error Messages

All phase lock error messages can result from improper front panel connections.

NO IF FOUND: CHECK R INPUT LEVEL means no IF was detected during pretune: a source problem. Perform the "A4 Sampler/Mixer Check".

NO PHASE LOCK: CHECK R INPUT LEVEL means the IF was not acquired after pretune: a source problem. Perform the "A4 Sampler/Mixer Check", earlier in this chapter.

PHASE LOCK CAL FAILED means that a calculation of pretune values was not successful: a source or receiver failure. Perform the "Source Pretune Correction Constants" routine as outlined in Chapter 3, "Adjustments and Correction Constants." If the analyzer fails that routine, perform the "A4 Sampler/Mixer Check".

PHASE LOCK LOST means that phase lock was lost or interrupted before the band sweep ended: a source problem. Refer to "Phase Lock Diagnostic Routines" next to access the phase lock loop diagnostic service routine. Then troubleshoot the problem by following the procedures in this chapter.

Phase Lock Diagnostic Routines

Perform the following steps to determine at what frequencies and bands the phase lock problem occurs.

1. Press **[System] [SERVICE MENU] [SERVICE MODES] [PLL AUTO OFF]** to switch off the automatic phase-locked loop. Normally, when the phase-locked loop detects lock problems, it automatically aborts the sweep and attempts to recalibrate the pretune cycle. Switching off PLL AUTO defeats this routine.
2. Press **[PLL DIAG ON]** to switch on the phase-locked loop diagnostic service mode. In this mode, the phase lock cycle and subsweep number are displayed on the analyzer display. (See "Service modes menu" in Chapter 10, "Service Key Menus and Error Messages", for more information.)
3. Press **[PLL PAUSE]** to pause the phase lock sequence and determine where the source is trying to tune when lock is lost.

Refer to "Source theory" in Chapter 12, "Theory of Operation", for additional information regarding band related problems. Then use the procedures in this chapter to check source functions at specific frequencies.

Broadband Power Problems

This section assumes that a power problem exists across the full frequency range, but that no error message is displayed on the analyzer. The problem may effect port 1, port 2, or both. Assemblies in question include:

- A3 source
- A21, A22 directional couplers
- A24 solid-state transfer switch
- any cables from the A3 source to the outputs of port 1 or port 2

8

Receiver Troubleshooting

Use this procedure only if you have read Chapter 4, "Start Troubleshooting Here." Follow the procedures in the order given, unless instructed otherwise.

The receiver group assemblies consist of the following:

- A4/5/6 sampler/mixer assemblies
- A10 digital IF assembly

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 87533 network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Receiver Failure Error Messages

The error messages which indicate receiver group problems may be caused by the instrument itself or by external devices or connections. The following three error messages share the same description.

- CAUTION: OVERLOAD ON INPUT A, POWER REDUCED
- CAUTION: OVERLOAD ON INPUT B, POWER REDUCED
- CAUTION: OVERLOAD ON INPUT R, POWER REDUCED

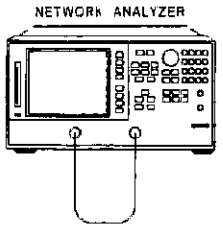
If any of the above error messages appear, the analyzer has exceeded approximately + 14 dBm at one of the test ports. The RF output power is automatically reduced to -85 dBm. The annotation P↓ appears in the left margin of the display to indicate that the power trip function has been activated. To reset the analyzer's power and regain control of the power level, do the following:

1. Remove any devices under test which may have contributed excess power to the input.
2. Press **[Menu] [POWER] [0] [x1] [SOURCE POWER ON]** to return the power level to the preset state.
   - If the power trip indicator (P↓) does not reappear, reconfigure the test setup to keep input power levels at 0 dBm or below.
   - If P↓ reappears, continue with "Check the A and B Inputs".

Check the A and B Inputs

Good inputs produce traces similar to Figure 8-2 in terms of flatness. To examine both input traces, do the following:

1. Connect the equipment as shown in Figure 8-1. (The through cable is HP part number 8120-4779.)



pg637a

Figure 8-1. Equipment Setup

2. Check the flatness of the input A trace by comparing it with the trace in Figure 8-2

   Press **[Preset] [Meas] [INPUT PORTS] [A] [TEST PORT 2] [Scale Ref] [AUTO SCALE].**

3. Check the flatness of the input B trace by comparing it with the trace in Figure 8-2

   Press **[Meas] [INPUT PORTS] [TEST PORT 1] [B].**

   - If neither of the input traces resembles Figure 8-2, continue with "Troubleshooting When All Inputs Look Bad".
   - If at least one input trace resembles Figure 8-2, continue with "Troubleshooting When One or More Inputs Look Good".

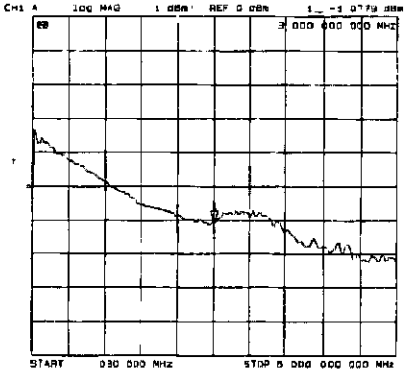


Figure 8-2. Typical Good Trace

Troubleshooting When All Inputs Look Bad

Run Internal Tests 18 and 17

1. Press **[Preset] [System] [SERVICE MENU] [TESTS] [18] [x1] [EXECUTE TEST]** to run. the ADC offset.
2. Then, when the analyzer finishes test 18, press **[17] [x1] [EXECUTE TEST]** to run the ADC linearity test.

If either of these tests FAIL, the A10 assembly is probably faulty. This can be confirmed by checking the 4 MHz signal and substituting the A10 assembly or checking the signals listed in

Check 2nd LO

Check the 2nd LO signal. Refer to the "A12 Reference Check" section of Chapter 7, "Source Troubleshooting" for analog bus and oscilloscope checks of the 2nd LO and waveform illustrations.

- If the analyzer passes the checks, continue to "Check the 4 MHz REF Signal".
- If the analyzer fails the checks, perform the high/low band transition adjustment If the adjustment fails, or brings no improvement, replace A12.

Check the 4 MHz REF Signal

1. Press **[Preset]**
2. Use an oscilloscope to observe the 4 MHz reference signal at A10P2-6.
   - If the signal does not resemble Figure 8-3, troubleshoot the signal source (A12P2-36) and path
   - If the signal is good, the probability is greater than 90% that the A10 assembly is faulty. For confirmation, perform "Check A10 by Substitution or Signal Examination".

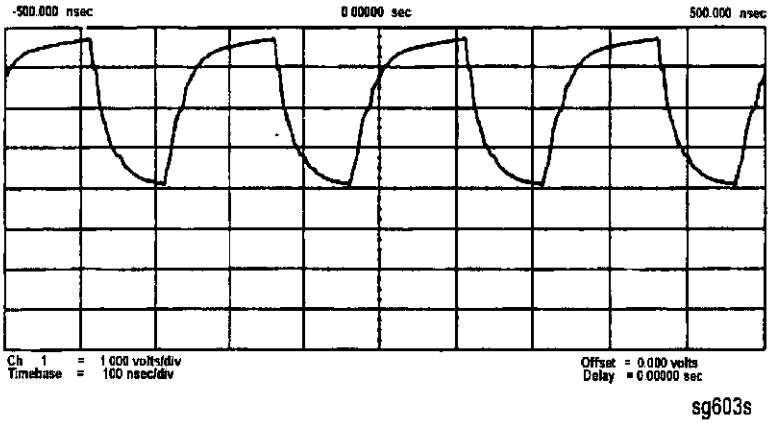


Figure 8-3. 4 MHz REF Waveform

Check A10 by Substitution or Signal Examination

If the 4 MHz REF signal is good at the A10 digital IF assembly, check the A10 assembly by one of the following methods:

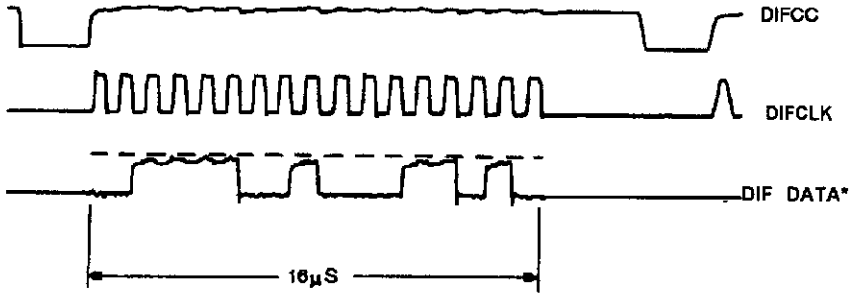
- Substitute another A10 assembly or
- Check the signal/control lines required for its operation. The pins and signal sources of those lines are identified in Table 8-1. It is possible that the A9 assembly may not be providing the necessary signals. These signal checks allow you to determine which assembly is faulty. Some of the waveforms are illustrated by Figure 8-4 and Figure 8-5.

If the substitute assembly shows no improvement or if all of the input signals are valid, continue with "Check the 4 kHz Signal". Otherwise troubleshoot the suspect signal(s) or consider the A10 assembly faulty.

Table 8-1. Signals Required for A10 Assembly Operation

Mnemonic	Description	A10 Location	Signal Source	See Figure
DIFD0	Digital IF data 0 (LSB)	P2-27	A9P2-27	*
DIFD1	Digital IF data 1	P2-57	A9P2-57	*
DIFD2	Digital IF data 2	P2-28	A9P2-28	*
DIFD3	Digital IF data 3	P2-58	A9P2-58	*
DIFD4	Digital IF data 4	P2-29	A9P2-29	*
DIFD5	Digital IF data 5	P2-59	A9P2-59	*
DIFD6	Digital IF data 6	P2-30	A9P2-30	*
DIFD7	Digital IF data 7 (MSB)	P2-60	A9P2-60	*
L DIFEN0	Digital IF enable 0	P2-34	A9P2-34	*
L DIFEN1	Digital IF enable 1	P2-5	A9P2-5	*
L DIFEN2	Digital IF enable 2	P2-35	A9P2-35	*
DIFCC	Digital IF conversion comp.	P2-33	A10P2-33	Figure 8-4
DIFCLK	Digital IF serial clock	P2-4	A10P2-4	Figure 8-4
DIF DATA	Digital IF serial data out	P2-3	A10P2-3	Figure 8-4
L ENDIF	L=enable digital IF	P2-17	A9P2-17	Figure 8-5
L INTCOP	L-interrupt, DSP	P2-2	A10P2-2	Figure 8-5

* Check for TTL activity



* DIF DATA consists of 16 serial bits per input conversion.
the LSB is on the right side and is the most volatile.

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Figure 8-4. Digital Data Lines Observed Using L INTCOP as Trigger

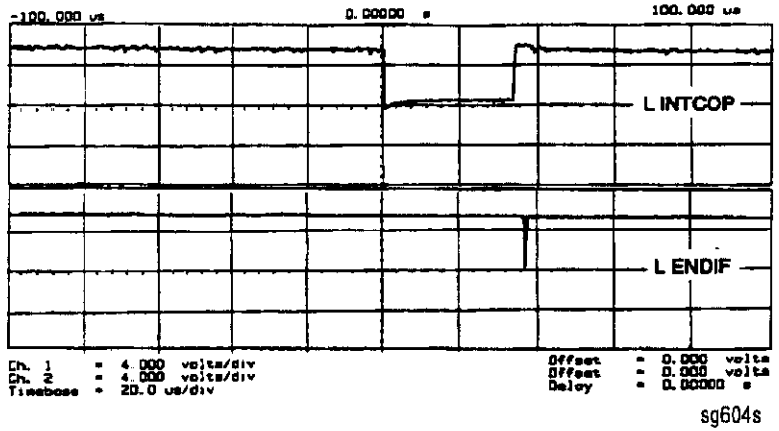

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Figure 8-5. Digital Control Lines Observed Using L INTCOP as Trigger

Troubleshooting When One or More Inputs Look Good

Since at least one input is good, all of the common receiver circuitry beyond the multiplexer is functional. Only the status of the individual sampler/mixers and their individual signal paths is undetermined.

Check the 4 kHz Signal

1. Press **[Preset] [Menu] [CW FREQ].**

2. Use an oscilloscope to check the 4 kHz output of the sampler/mixer in question at the A10 assembly. The input and output access pins are listed in Table 8-2. The signal should resemble the waveform of Figure 8-6.

   - If the signal is good, continue with "Check the Trace with the Sampler Correction Constants Off ".
   - If the signal is bad, skip ahead to "Check 1st LO Signal at Sampler/Mixer".

Table 8-2. 2nd IF (4 kHz) Signal Locations

Mnemonic	Description	A10 Location	Signal Source
IFR	4 kHz	A10P1-1, 31	A4P1-6
IFA	4 kHz	A10P1-4, 34	A5P1-6
IFB	4 kHz	A10P1-7, 37	A6P1-6

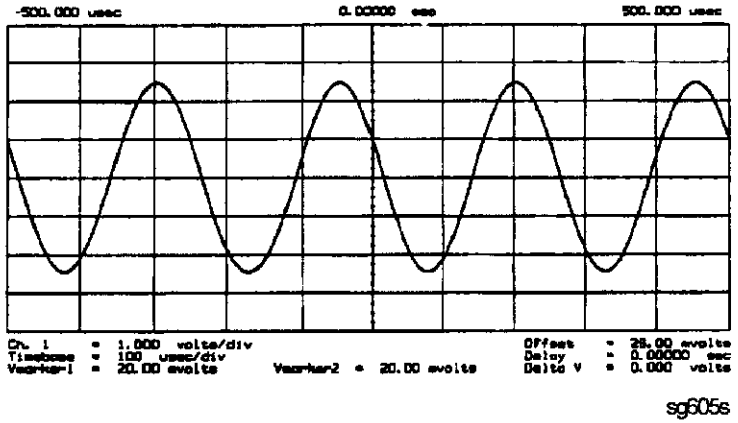

Figure 8-6. 2nd IF (4 kHz) Waveform

Check the Trace with the Sampler Correction Constants Off

1. Press **[Preset] [Meas] [INPUT PORTS] [A] [Scale Ref] [AUTO SCALE].**
2. The trace is currently being displayed with the sampler correction constants on and should resemble Figure 8-7a.
3. Press **[System] [SERVICE MENU] [SERVICE MODES] [MORE] [SAMPLER COR OFF].**
4. The trace is now being displayed with sampler correction constants off and should have worsened to resemble Figure 8-7b.
5. Press **[SAMPLER COR ON].** The trace should improve and resemble Figure 8-7a again.

Note When the correction constants are switched off, an absolute offset and bandswitch points may be evident.

If the trace shows no improvement when the sampler correction constants are toggled from off to on, perform the "Sampler Magnitude and Phase Correction Constants (Test 53)" adjustment described in Chapter 3, "Adjustments and Correction Constants." If the trace remains bad after this adjustment, the A10 assembly is defective.

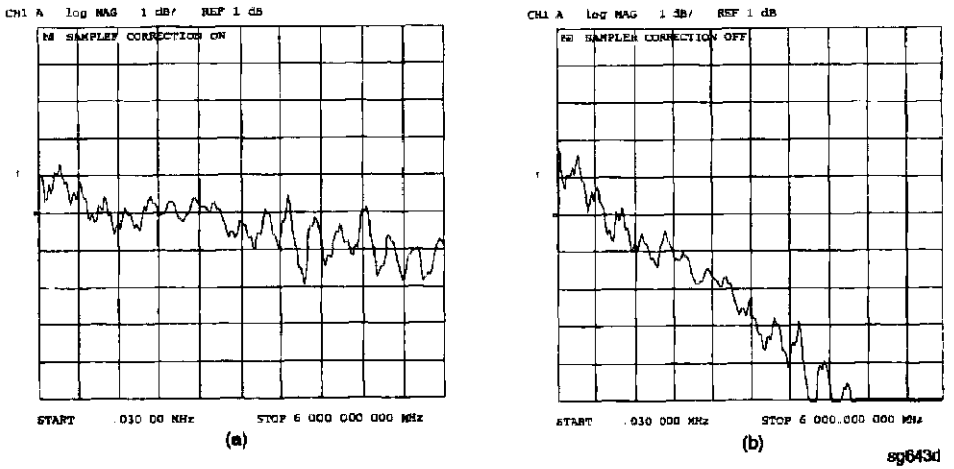

Figure 8-7. Typical Trace with Sampler Correction On and Off

Check 1st LO Signal at Sampler/Mixer

If the 4 kHz signal is bad at the sampler/mixer assembly, check the 1st LO signal where it enters the sampler/mixer assembly in question.

- If the 1st LO is faulty, check the 1st LO signal at its output connector on the A7 assembly to determine if the failure is in the cable or the assembly.
- If the 1st LO is good, continue with "Check 2nd LO Signal at Sampler/Mixer".

Check 2nd LO Signal at Sampler/Mixer

Check the 2nd LO signal at the pins identified in Table 8-3. Refer to the "A12 Reference Check" in Chapter 7, "Source Troubleshooting", for analog bus and oscilloscope checks of the 2nd LO and waveform illustrations. Table 8-3 identifies the signal location at the samplers and the A12 assembly.

Table 8-3. 2nd LO Locations

Mnemonic	Description	Sampler Location	Signal Source
2nd LO 1	2nd LO (0 degrees)	A4/5/6 P1-11	A12P1-2, 32
2nd LO 2	2nd LO (−90 degrees)	A4/5/6 P1-4	A12P1-4, 34

If the 2nd LO is good at the sampler/mixer, the sampler/mixer assembly is faulty. Otherwise, troubleshoot the A12 assembly and associated signal path.

9

Accessories Troubleshooting

Use this procedure only if you have read Chapter 4, "Start Troubleshooting Here." Follow the procedures in the order given, unless instructed otherwise.

Measurement failures can be divided into two categories:

- Failures which don't affect the normal functioning of the analyzer but render incorrect measurement data.
- Failures which impede the normal functioning of the analyzer or prohibit the use of a feature.

This chapter addresses the first category of failures which are usually caused by the following:

- operator errors
- faulty calibration devices or connectors
- bad cables or adapters
- improper calibration techniques

These failures are checked using the following procedures:

- "Inspect the Accessories"
- "Inspect the Error Terms"

Assembly Replacement Sequence

The following steps show the sequence to replace an assembly in an HP 8753E network analyzer

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Inspect the Accessories

Inspect the Test Port Connectors and Calibration Devices

1. Check for damage to the mating contacts of the test port center conductors and loose connector bulkheads.
2. Inspect the calibration kit devices for bent or broken center conductors and other physical damage. Refer to the calibration kit operating and service manual for information on gaging and inspecting the device connectors.

   If any calibration device is obviously damaged or out of mechanical tolerance, replace the device.

Inspect the Error Terms

Error terms are a measure of a "system": a network analyzer, calibration kit, and any cables used. As required, refer to Chapter 11, "Error Terms, " for the following:

- The specific measurement calibration procedure used to generate the error terms.
- The routines required to extract error terms from the instrument.
- Typical error term data.

Use Table 9-1 to cross-reference error term data to system faults.

Table 9-1. Components Related to Specific Error Terms

Component	Directivity	Source Match	Reflection Tracking	Isolation	Load Match	Transmission Tracking
Calibration Kit						
load	X					
open/short	X	X				
Analyzer						
sampler			X	X		X
A10 digital IF				X		
test port connectors	X	X	X	X	X	X
External cables					X	X

If you detect problems using error term analysis, use the following approach to isolate the fault:

1 Check the cable by examining the load match and transmission tracking terms. If those terms are incorrect, go to "Cable Test."

2. Verify the calibration kit devices:

   Loads: If the directivity error term looks good, the load and the test port are good. If directivity looks bad, connect the same load on the other test port and measure its directivity. If the second port looks bad, as if the problem had shifted with the load, replace the load. If the second port looks good, as if the load had not been the problem, troubleshoot the first port.

   Shorts and opens: If the source match and reflection tracking terms look good, the shorts and the opens are good. If these terms look bad while the rest of the terms look good, proceed to "Verify Shorts and Opens."

Cable Test

The load match error term is a good indicator of cable problems. You can further verify a faulty cable by measuring the reflection of the cable. Perform an S11 1-port calibration directly at port 1 (no cables). Then connect the suspect cable to port 1 and terminate the open end in 50 ohms.

Figure 9-1 shows the return loss trace of a good (left side) and faulty cable. Note that the important characteristic of a cable trace is its level (the good cable trace is much lower) not its regularity. Refer to the cable manual for return loss specifications.

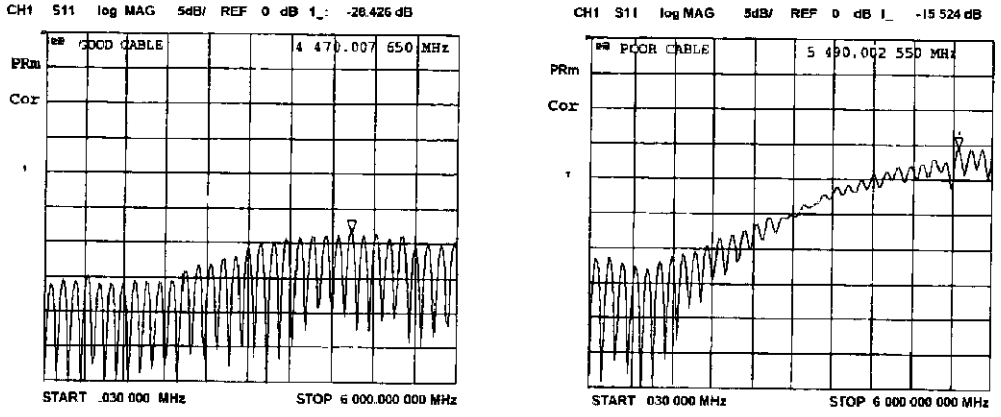

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Figure 9-1. Typical Return Loss Traces of Good and Poor Cables

Verify Shorts and Opens

Substitute a known good short and open of the same connector type and sex as the short and open in question. If the devices are not from one of the standard calibration kits, refer to the *HP 8753E Network Analyzer User's Guide* for information on how to use the **[MODIFY CAL KIT]** function. Set aside the short and open that are causing the problem.

1. Perform an S11 1-port calibration using the good short and open. Then press **[FORMAT] [SMITH CHART]** to view the devices in Smith chart format.

2. Connect the good short to port 1. Press **[Scale Ref] [ELECTRICAL DELAY]** and turn the front panel knob to enter enough electrical delay so that the trace appears as a dot at the left side of the circle. (See Figure 9-2a, left.)

   Replace the good short with the questionable short at port 1. The trace of the questionable short should appear very similar to the known good short.

3. Connect the good open to port 1. Press **[Scale Ref] [ELECTRICAL DELAY]** and turn the front panel knob to enter enough electrical delay so that the trace appears as a dot at the right side of the circle. (See Figure 9-2b, right.)

   Replace the good open with the questionable open at port 1. The trace of the questionable open should appear very similar to the known good open.

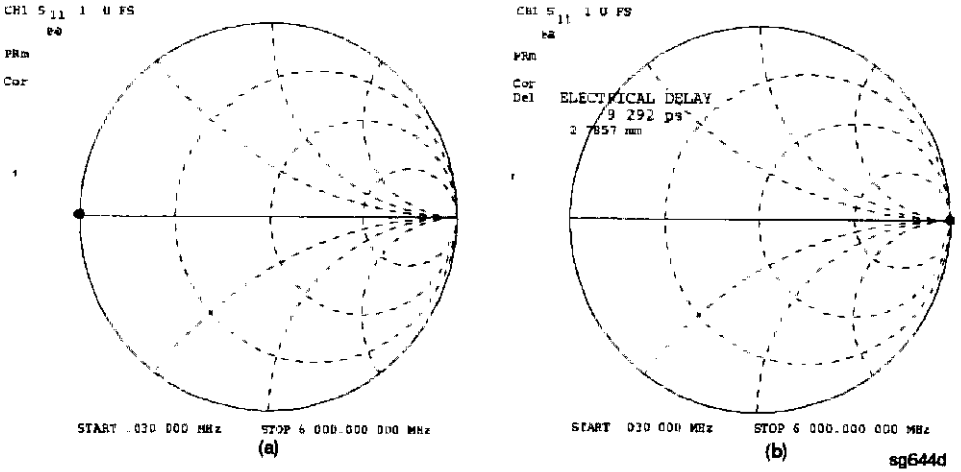


Figure 9-2. Typical Smith Chart Traces of Good Short (a) and Open (b)

10

Service Key Menus and Error Messages

Service Key Menus

These menus allow you to perform the following service functions:

- test
- verify
- adjust
- control
- troubleshoot

The menus are divided into two groups:

1. Internal Diagnostics
2. Service Features

When applicable, the HP-IB mnemonic is written in parentheses following the key. See HP-IB Service Mnemonic Definitions at the end of this section.

Error Messages

The displayed messages that pertain to service functions are also listed in this chapter to help you:

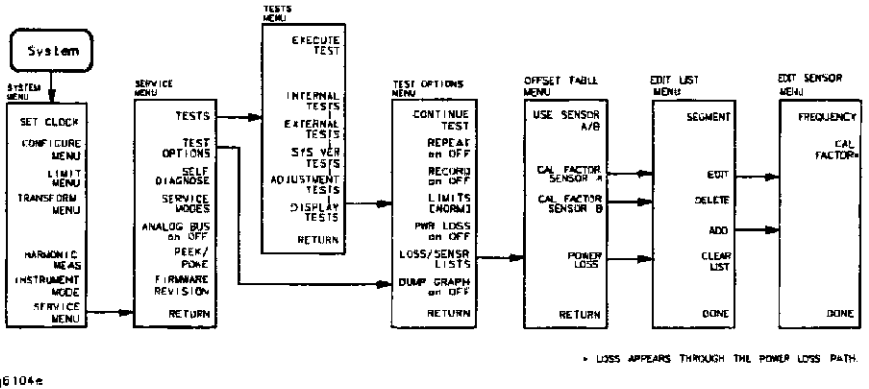
- Understand the message.

- Solve the problem.

Service Key Menus - Internal Diagnostics

The internal diagnostics menus are shown in Figure 10-1 and described in the following paragraphs. The following keys access the internal diagnostics menus:

- TESTS
- TEST OPTIONS
- [SELF-DIAGNOSE]



sg6104e

Figure 10-1. Internal Diagnostics Menus

Note

Throughout this service guide, these conventions are observed:

- **[HARDKEYS]** are labeled front panel keys.
- **[SOFTKEYS]** are display defined keys (in the menus).
- **(HP-IB COMMANDS)** when applicable, follow the keystrokes in parentheses.

Tests Menu

To access this menu, press **[System] [SERVICE MENU] [TESTS].**

TESTS (TEST [D]) accesses a menu that allows you to select or execute the service tests. The default is set to internal test 1.

Note Descriptions of tests in each of the categories are given under the heading Test Descriptions in the following pages.

The tests are divided by function into the following categories.

- Internal Tests (0-20)
- External Tests (21-26)
- System Verification Tests (27-43)
- Adjustment Tests (44-58)
- Display Tests (59-65)
- Test Patterns (66-80)

To access the first test in each category, press the category softkey. To access the other tests, use the numeric keypad, step keys, or front panel knob. The test number, name, and status abbreviation will be displayed in the active entry area of the display.

Table 10-1 shows the test status abbreviation that appears on the display, its definition, and the equivalent HP-IB code. The HP-IB command to output the test status of the most recently executed test is OUTPTESS. For more information, refer to "HP-1B Service Mnemonic Definitions" located at the end of this chapter.

Table 10-1. Test Status Terms

Display Abbreviation	Definition	HP-IB Code
PASS	PASS	0
FAIL	FAIL	1
-IP-	IN PROGRESS	2
(NA)	NOT AVAILABLE	3
-ND-	NOT DONE	4
DONE	DONE	5

[EXECUTE TEST] (EXET) runs the selected test and may display these softkeys:

[CONTINUE] (TESR1) continues the selected test.

[YES] (TESR2) alters correction constants during adjustment tests.

[NEXT] (TESR4) displays the next choice.

[SELECT] (TESR6) chooses the option indicated.

[ABORT] (TESR8) terminates the test and returns to the tests menu.

[INTERNAL TESTS] evaluates the analyzer's internal operation These tests are completely internal and do not require external connections or user interaction

[EXTERNAL TESTS] evaluate the analyzer' s external operation. These additional tests require some user interaction (such as keystrokes).

[SYS VER TESTS] verifies the analyzer system operation by examining the contents of the measurement calibration arrays. The procedure is in the "System Verification and Performance Tests" chapter. Information about the calibration arrays is provided in the "Error Terms" chapter.

[ADJUSTMENT TESTS] generates and stores the correction constants. For more information, refer to the "Adjustments" chapter.

[DISPLAY TESTS] checks for correct operation of the display and GSP board.

Test Options Menu

To access this menu, press **[System] [SERVICE MENU] [TEST OPTIONS].**

[TEST OPTIONS] accesses softkeys that affect the way tests (routines) run, or supply necessary additional data.

[CONTINUE TEST] (TESR1) resumes the test from where it was stopped.

[REPEAT on OFF] (T02) toggles the repeat function on and off. When the function is ON, the selected test will run 10,000 times unless you press any key to stop it. The analyzer shows the current number of passes and fails.

[RECORD on OFF] (T01) toggles the record function on and off. When the function is ON, certain test results are sent to a printer via HP-IB. This is especially useful for correction constants. The instrument must be in system controller mode or pass control mode to print (refer to the "Printing, Plotting, and Saving Measurement Results" chapter in the ***HP 8753E User's Guide.***

[LIMITS [NORM/SPCL]] selects either NORMal or SPeCiaL (tighter) limits for the Operator's Check. The SPCL limits are useful for a guard band.

[PWR LOSS] (POWLLIST) accesses the following Edit List menu to allow modification of the external power loss data table.

[LOSS/SENSR LISTS] accesses the power loss/sensor lists menu:

[USE SENSOR A/B] selects the A or B power sensor calibration factor list for use in power meter calibration measurements.

[CAL FACTOR SENSOR A] (CALFSENA) accesses the Edit List menu to allow modification of the calibration data table for power sensor A.

[CAL FACTOR SENSOR B] (CALFSENB) accesses the Edit List menu to allow modification of the calibration data table for power sensor B.

[POWER LOSS] (POWLLIST) accesses the Edit List menu to allow modification of the external power loss data table that corrects coupled-arm power loss when a directional coupler samples the RF output.

[DUMP GRAPH] generates printed graphs of verification results when activated during a system verification.

Edit List Menu To access this menu, press **[System] [SERVICE MENU] [TEST OPTIONS] [LOSS/SENSR LISTS]** and then press one of the following: **[CAL FACTOR SENSOR A]** or **[CAL FACTOR SENSOR B]** or **[POWER LOSS].**

[SEGMENT] selects a segment (frequency point) to be edited, deleted from, or added to the current data table. Works with the entry controls.

[EDIT] (SEDI[D|) allows modification of frequency, cal factor and loss values previously entered in the current data table.

[DELETE] (SDEL) deletes frequency, cal factor and loss values previously entered in the current data table.

[ADD] (SADD) adds new frequency, cal factor and loss values to the current data table up to a maximum of 12 segments (frequency points, PTS).

[CLEAR LIST] (CLEL) deletes the entire current data table (or list) when **[YES]** is pressed. Press **[NO]** to avoid deletion.

[DONE] (EDITDONE) returns to the previous menu.

Self Diagnose Softkey

You can access the self diagnosis function by pressing, **[System] [SERVICE MENU] [SELF DIAGNOSE]**. This function examines, in order, the pass/fail status of all internal tests and displays NO FAILURE FOUND if no tests have failed.

If a failure is detected, the routine displays the assembly or assemblies most probably faulty and assigns a failure probability factor to each assembly.

Test Descriptions

The analyzer has up to 80 routines that test, verify, and adjust the instrument. This section describes those tests

Internal Tests

This group of tests runs without external connections or operator interaction. All return a PASS or FAIL condition. All of these tests run on power-up and PRESET except as noted.

0 **ALL INT**. Runs only when selected. It consists of internal tests 3-11, 13-16, and 20. Use the front panel knob to scroll through the tests and see which failed. If all pass, the test displays a PASS status. Each test in the subset retains its own test status.

1 **PRESET**. Runs the following subset of internal tests: first, the ROM/RAM tests 2, 3, and 4; then tests 5 through 11, 14, 15, and 16. If any of these tests fail, this test returns a FAIL status. Use the front panel knob to scroll through the tests and see which failed. If all pass, this test displays a PASS status. Each test in the subset retains its own test status. This same subset is available over HP-IB as "TST?". It is not performed upon remote preset.

2 **ROM**. Part of the ROM/RAM tests and cannot be run separately. Refer to the "Digital Control Troubleshooting" chapter for more information.

3 **SRAM RAM.** Verifies the A9 CPU SRAM (long-term) memory with a non-destructive write/read pattern. A destructive version that writes over stored data at power-on can be enabled by changing the 4th switch position of the A9 CPU switch as shown in Figure 10-2.

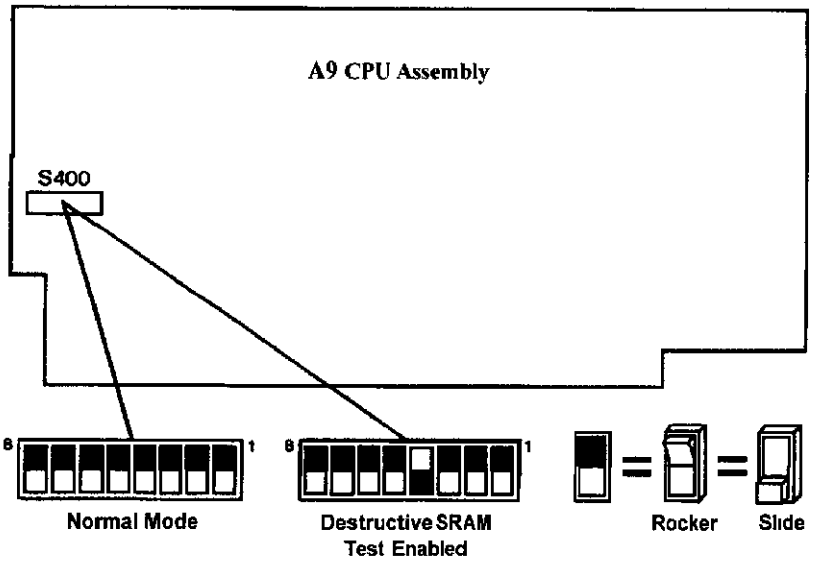


Figure 10-2. A9 CPU Switch Positions

4 **Main DRAM.** Verifies the A9 CPU main memory (DRAM) with a non-destructive write/read test pattern. A destructive version of this test is run during power-on.

For additional information, see Internal Tests (near the front of this section) and the "Digital Control Troubleshooting" chapter.

5. **DSP Wr/Rd.** Verifies the ability of the main processor and the DSP (digital signal processor), both on the A9 CPU assembly, to communicate with each other through DRAM. This also verifies that programs can be loaded to the DSP, and that most of the main RAM access circuits operate correctly.

6. **DSP RAM.** Verifies the A9 CPU RAM associated with the digital signal processor by using a write/read pattern.

7. **DSP ALU.** Verifies the A9 CPU high-speed math processing portions of the digital signal processor.

8. **DSP Intrpt.** Tests the ability of the A9 CPU digital signal processor to respond to interrupts from the A10 digital IF ADC.

9. **DIF Control.** Tests the ability of the A9 CPU main processor to write/read to the control latches on the A10 digital IF.

10. **DIF Counter.** Tests the ability of the A9 CPU main processor to write/read to the triple divider on the A10 CPU. It tests the A9 CPU data buffers and A10 digital IF, the 4 MHz clock from the A12 reference.

11. **DSP Control.** Tests the ability of the A9 CPU digital signal processor to write to the control latches on the A10 digital IF Feedback is verified by the main processor. It primarily tests the A10 digital IF, but failures may be caused by the A9 CPU.

12. **Fr Pan Wr/Rd.** Tests the ability of the A9 CPU main processor to write/read to the front panel processor. It tests the A2 front panel interface and processor, and A9 CPU data buffering and address decoding. (See also tests 23 and 24.) This runs only when selected.

13. **Rear Panel.** Tests the ability of the A9 CPU main processor to write/read to the rear panel control elements. It tests the A16 rear panel, and A9 CPU data buffering and address decoding. (It does not test the HP-IB interface; for that, see the HP-IB Programming Guide.) This runs only when selected or with ALL INTERNAL.

14. **Post Reg.** Polls the status register of the A8 post-regulator, and flags these conditions: heat sink too hot, inadequate air flow, or post-regulated supply shutdown.

15 **Frac N Cont.** Tests the ability of the A9 CPU main processor to write/read to the control element on the Al4 fractional-N (digital) assembly. The control element must be functioning, and the fractional-N VCO must be oscillating (although not necessarily phase-locked) to pass.

16 **Sweep Trig.** Tests the sweep trigger (L SWP) line from the Al4 fractional-N to the A10 digital IF. The receiver with the sweep synchronizes L SWP

17 **ADC Lin. It** tests the linearity of the Al0 digital IF ADC using the built-in ramp generator. The test generates a histogram of the ADC linearity, where each data point represents the relative "width" of a particular ADC code. Ideally, all codes have the same width; different widths correspond to non-linearities.

18 **ADC Ofs.** This runs only when selected. It tests the ability of the offset DAC, on the A10 digital IF, to apply a bias offset to the IF signals before the ADC input. This runs only when selected.

19 **ABUS Test.** Tests analog bus accuracy, by measuring several analog bus reference voltages (all nodes from the A10 digital IF). This runs only when selected.

20 **FN Count.** Uses the internal counter to count the Al4 fractional-N VCO frequency (120 to 240 MHz) and the divided fractional-N frequency (100 kHz). It requires the 100 kHz signal from Al2 and the counter gate signal from A10 to pass.

External Tests

These tests require either external equipment and connections or operator interaction of some kind to run. Tests 30 and 60 are comprehensive front panel checks, more complete than test 12, that checks the front panel keys and knob entry.

21 **Port 1 Op Chk.** Part of the "Operator's Check" procedure, located in the "Start Troubleshooting" chapter. The procedure requires the external connection of a short to PORT 1.

22 **Port 2 Op Chk.** Same as 21, but tests PORT 2.

23 **Fr Pan Seq.** Tests the front panel knob entry and all A1 front panel keys, as well as the front panel microprocessor on the A2 assembly. It prompts the user to rotate the front panel knob, then press each key in an ordered sequence. It continues to the next prompt only if the current prompt is correctly satisfied.

24 **Fr Pan Diag.** Similar to 23 above, but the user rotates the front panel knob or presses the keys in any order. This test displays the command the instrument received.

25 **ADC Hist.** Factory use only.

26 **Source Ex.** Factory use only.

System Verification Tests

These tests apply mainly to system-level, error-corrected verification and troubleshooting. Tests 27 to 31 are associated with the system verification procedure, documented in the "System Verification and Performance Tests" chapter. Tests 32 to 43 facilitate examining the calibration coefficient arrays (error terms) resulting from a measurement calibration; refer to the "Error Terms" chapter for details.

27 **Sys Ver Init.** Recalls the initialization state for system verification from an HP 8753E verification disk, in preparation for a measurement calibration. It must be done before service internal tests 28, 29, 30, or 31 are performed.

28 **Ver Dev 1.** Recalls verification limits from disk for verification device #1 in all applicable S-parameter measurements. It performs pass/fail limit testing of the current measurement.

29 **Ver Dev 2**. Same as 28 above for device #2

30 **Ver Dev 3.** Same as 28 above for device #3.

31 **Ver Dev 4.** Same as 28 above for device #4.

32-43 **Cal Coef 1-12.** Copies error term data from a measurement calibration array to display memory. A measurement calibration must be complete and active. The definition of calibration arrays depends on the current calibration type. After execution, the memory is automatically displayed. Refer to the "Error Term" chapter for details.

Adjustment Tests

The tests without asterisks are used in the procedures located in the "Adjustments" chapter of this manual, except as noted.

44 ***Source Def.** Writes default correction constants for rudimentary source power accuracy. Use this test before running test 47, below.

45 ***Pretune Def.** Writes default correction constants for rudimentary phase lock pretuning accuracy. Use this test before running test 48, below.

46 **ABUS Cor.** Measures three fixed voltages on the ABUS, and generates new correction constants for ABUS amplitude accuracy in both high resolution and low resolution modes. Use this test before running test 48, below.

47 **Source Cor.** Measures source output power accuracy, flatness, and linearity against an external power meter via HP-IB to generate new correction constants. Run tests 44, 45, 46, and 48 first.

48 **Pretune Cor.** Generates source pretune values for proper phase-locked loop operation. Run tests 44, 45, and 46 first.

50 **Disp 2 Ex.** Not used in "Adjustments." Writes the "secondary test pattern" to the display for adjustments. Press **[Preset]** to exit this routine.

51 **IF Step Cor.** Measures the gain of the IF amplifiers (A and B only) located on the A10 digital IF, to determine the correction constants for absolute amplitude accuracy. It provides smooth dynamic accuracy and absolute amplitude accuracy in the -30 dBm input power region.

52 **ADC Ofs Cor.** Measures the A10 Digital IF ADC linearity characteristics, using an internal ramp generator, and stores values for the optimal operating region. During measurement, IF signals are centered in the optimal region to improve low-level dynamic accuracy.

53 **Sampler Cor.** Measures the absolute amplitude response of the R sampler against an external power meter via HP-IB, then compares A and B, (magnitude and phase), against R. It improves the R input accuracy and A/B/R tracking.

54 **Cav Osc Cor.** Calculates the frequency of the cavity oscillator and the instrument temperature for effective spur avoidance.

55 **Serial Cor.** Stores the serial number (input by the user in the Display Title menu) in EEPROM. This routine will not overwrite an existing serial number.

56 **Option Cor.** Stores the option keyword (required for Option 002, 006, 010 or any combination).

57 **Not used.**

58 **Init EEPROM.** This test initializes certain EEPROM addresses to zeros and resets the display intensity correction constants to the default values. Also, the test will not alter the serial number and correction constants for Option 002, 006, and 010.

Display Tests

These tests return a PASS/FAIL condition. All six amber front panel LEDs will turn off if the test passes. Press **[Preset]** to exit the test If any of the six LEDs remain on, the test has failed.

59 **Disp/cpu corn.** Checks to confirm that the CPU can communicate with the A19 GSP board. The CPU writes all zeros, all ones, and then a walking one pattern to the GSP and reads them back. If the test fails, the CPU repeats the walking 1 pattern until **[Preset]** is pressed.

60 **DRAM cell.** Tests the DRAM on A19 by writing a test pattern to the DRAM and then verifying that it can be read back.

61 **Main VRAM.** Tests the VRAM by writing all zeros to one location in each bank and then writing all ones to one location in each bank. Finally a walking one pattern is written to one location in each bank.

62 **VRAM bank.** Tests all the cells in each of the 4 VRAM banks.

63 **VRAM/video.** Verifies that the GSP is able to successfully perform both write and read shift register transfers. It also checks the video signals LHSYNC, LVSYNC, and LBLANK to verify that they are active and toggling.

64 **RGB outputs.** Confirms that the analog video signals are correct and it verifies their functionality.

65 **Inten DAC.** Verifies that the intensity DAC can be set both low and high.

Test Patterns

Test patterns are used in the factory for display adjustments, diagnostics, and troubleshooting, but they are not used for field service. Test patterns are executed by entering the test number (66 through SO), then pressing **[EXECUTE TEST] [CONTINUE].** The test pattern will be displayed and the softkey labels blanked. To increment to the next pattern, press softkey 1; to go back to a previous pattern, press softkey 2. To exit the test pattern and return the softkey labels, press softkey 8 (bottom softkey). The following is a description of the test patterns.

66 **Test Pat 1.** Displays an all white screen for verifying the light output of the A18 display and checks for color purity.

67-69 **Test Fat 2-4.** Displays a red, green, and blue pattern for verifying the color purity of the display and also the ability to independently control each color.

70 **Test Pat 5.** Displays an all black screen. This is used to check for stuck pixels.

71 **Test Pat 6.** Displays a 16-step gray scale for verifying that the A19 GSP board can produce 16 different amplitudes of color (in this case, white). The output comes from the RAM on the GSP board, it is then split. The signal goes through a video DAC and then to an external monitor or through some buffer amplifiers and then to the internal LCD display. If the external display looks good but the internal display is bad, then the problem may be with the display or the cable connecting it to the GSP board. This pattern is also very useful when using an oscilloscope for troubleshooting. The staircase pattern it produces will quickly show missing or stuck data bits.

72 **Test Pat 7.** Displays the following seven colors: Red, Yellow, Green, Cyan, Blue, Magenta and White.

73 **Test Pat 8.** This pattern is intended for use with an external display. The pattern displays a color rainbow pattern for showing the ability of the A19 GSP board to display 15 colors plus white. The numbers written below each bar indicate the tint number used to produce that bar (0 & 100=pure red, 33= pure green, 67= pure blue).

74 **Test Fat 9.** Displays the three primary colors Red, Green, and Blue at four different intensity levels. You should see 16 color bands across the screen. Starting at the left side of the display the pattern is: Black four bands of Red (each band increasing in intensity) Black four bands

of Green (each band increasing in intensity) Black four bands of Blue (each band increasing in intensity) Black If any one of the four bits for each color is missing the display will not look as described.

75 **Test Pat 10**. Displays a character set for showing the user all the different types and sizes of characters available. Three sets of characters are drawn in each of the three character sizes. 125 characters of each size are displayed. Characters 0 and 3 cannot be drawn and several others are really control characters (such as carriage return and line feed).

76 **Test Pat 11.** Displays a bandwidth pattern for verifying the bandwidth of the EXTERNAL display. It consists of multiple alternating white and black vertical stripes. Each stripe should be clearly visible. A limited bandwidth would smear these lines together. This is used to test the quality of the external monitor.

77 **Test Pat 12.** Displays a repeating gray scale for troubleshooting, using an oscilloscope. It is similar to the 16 step gray scale but is repeated 32 times across the screen. Each of the 3 outputs of the video palette will then show 32 ramps (instead of one staircase) between each horizontal sync pulse. This pattern is used to troubleshoot the pixel processing circuit of the A19 GSP board.

78 **Test Pat 13.** Displays a convergence pattern for measuring the accuracy of the color convergence of the external monitor.

79-80 **Test Fat 14-15.** Displays crosshatch and inverse crosshatch patterns for testing color convergence, linearity, and alignment. This is useful when aligning the LCD display in the bezel.

Service Key Menus - Service Features

The service feature menus are shown in Figure 10-3 and described in the following paragraphs. The following keys access the service feature menus:

- SERVICE MODES
- ANALOG BUS on OFF
- PEEK/POKE
- FIRMWARE REVISION

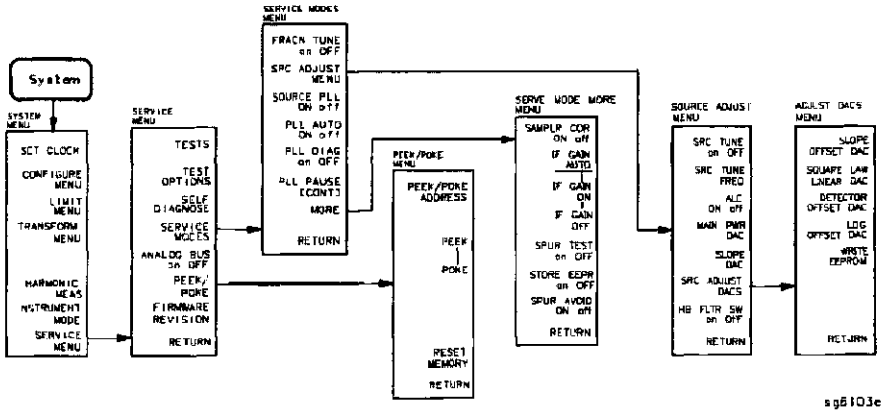


Figure 10-3. Service Feature Menus

Service Modes Menu

To access this menu, press: **[System] [SERVICE MENU] [SERVICE MODES]**

[SERVICE MODES] allows you to control and monitor various circuits for troubleshooting.

[FRACN TUNE on OFF] (SM1) tests the A13 and A14 fractional-N circuits. It allows you to directly control and monitor the output frequency of the fractional-N synthesizer (10 MHz to 60 MHz). Set the instrument to CW sweep mode and then set FRACN TUNE ON.

Change frequencies with the front panel keys or knob. The output of the A14 assembly can be checked at A14J1 HI OUT (in high band) or A14J2 LO OUT (in low band) with an oscilloscope, a frequency counter, or a spectrum analyzer. Signal jumps and changes in shape at 20 MHz and 30 MHz when tuning up in frequency, and at 29.2 MHz and 15 MHz when tuning down, are due to switching of the digital divider. This mode can be used with the SRC TUNE mode as described in "Source Troubleshooting" chapter.

[SRC ADJUST MENU] accesses the functions that allow you to adjust the source:

[SRC TUNE on OFF] tests the pretune functions of the phase lock and source assemblies. Use the entry controls to set test port output to any frequency from 300 KHz to 6 GHz When in this mode:

- Set analyzer to CW frequency before pressing **SRC TUNE ON**.
- Test port output is 1 to 6 MHz above indicated (entered) frequency.
- Instrument does not attempt to phase lock.
- Residual FM increases.

[SRC TUNE FREQ] allow you to change the source tune frequency.

[ALC ON off] toggles the automatic leveling control (ALC) on and off.

[MAIN PWR DAC]

[SLOPE DAC]

[SRC ADJUST DACS]

[HB FLTR SW on OFF]

[SOURCE PLL ON off] (SM3) With this mode switched OFF, the source stays in the pretune mode and does not attempt to complete the phase lock sequence. Also, all phase lock error messages are disabled. The fractional-N circuits and the receiver operate normally. Therefore, the instrument sweeps, but the source is being driven by the pretune DAC in a stair-stepped fashion.

[PLL AUTO ON off] (SM4) Automatically attempts to determine new pretune values when the instrument encounters phase lock problems (for example, "harmonic skip"). With **[PLL AUTO OFF]** the frequencies and voltages do not change, like when they are attempting to determine new pretune values, so troubleshooting the phase-locked loop circuits is more convenient. This function may also be turned off to avoid pretune calibration errors in applications where there is a limited frequency response in the R (reference) channel. For example, in a high power test application, using band limited filters for R channel phase locking.

[PLL DIAG on OFF] (SM5) displays a phase lock sequence at the beginning of each band. This sequence normally occurs very rapidly, making it difficult to troubleshoot phase lock problems. Switching this mode ON slows the process down, allowing you to inspect the steps of the phase lock sequence (pretune, acquire, and track) by pausing at each step. The steps are indicated on the display, along with the channel (C1 or C2) and band number (B1 through B13).

This mode can be used with PLL PAUSE to halt the process at any step. It can also be used with the analog bus counter

[PLL PAUSE] used only with PLL DIAG mode. **[CONT]** indicates that it will continuously cycle through all steps of the phase lock sequence. **[PAUSE]** holds it at any step of interest. This mode is useful for troubleshooting phase-locked loop problems.

MORE Accesses the service modes more menu listed below.

Service Modes More Menu

To access this menu, press **[System] [SERVICE MENU] [SERVICE MODES] [MORE].**

[SAMPLER COR ON off] (SM6) Toggles the sampler correction routine ON, for normal operation, or OFF, for diagnosis or adjustment purposes.

[IF GAIN AUTO] Normal operating condition and works in conjunction with IF GAIN ON and OFF. The A10 assembly includes a switchable attenuator section and an amplifier that amplifies low-level 4 kHz IF signals [for A and B inputs only). This mode allows the A10 IF section to automatically determine if the attenuator should be switched in or out. The switch occurs when the A or B input signal is approximately -30 dBm.

[IF GAIN ON] Locks out the A10 IF attenuator sections for checking the A10 IF gain amplifier circuits, regardless of the amplitude of the A or B IF signal. Switches out both the A and B attenuation circuits; they cannot be switched independently. Be aware that input signal levels above -30 dBm. at the sampler input will saturate the ADC and cause measurement errors.

[IF GAIN OFF] Switches in both of the A10 IF attenuators for checking the A10 IF gain amplifier circuits. Small input signals will appear noisy, and raise the apparent noise floor of the instrument.

[SPUR TEST on OFF] (SM7) For factory use only.

[STORE EEPR on OFF] Allows you to store the correction constants that reside in non-volatile memory (EEPROM) onto a disk. Correction constants improve instrument performance by compensating for specific operating variations due to hardware limitations (refer to the "Adjustments" chapter). Having this information on disk is useful as a backup, in case the constants are lost (due to a CPU board failure). Without a disk backup the correction constants can be regenerated

manually, although the procedures are more time consuming.

[SPUR AVOID ON off] (SM8) offsets the frequency of both the A3 YIG oscillator and the A3 cavity oscillator to avoid spurs which cannot otherwise be filtered out. **[SPUR AVOID OFF]** allows examination of these spurs for service,

[ANALOG BUS on OFF] (ANAB) enables and disables the analog bus, described below. Use it with the analog in menu, (a description of this menu follows).

Analog Bus

To access the analog bus, press **[System] [SERVICE MENU] [ANALOG BUS ON]**

Description of the Analog Bus

The analog bus is a single multiplexed line that networks 31 nodes within the instrument. It can be controlled from the front panel, or through HP-IB, to make voltage and frequency measurements just like a voltmeter, oscilloscope, or frequency counter. The next few paragraphs provide general information about the structure and operation of the analog bus. See "Analog Bus Nodes," for a description of each individual node. Refer to the "Overall Block Diagram," in the "Start Troubleshooting" chapter, to see where the nodes are located in the instrument.

The analog bus consists of a source section and a receiver section. The source can be the following:

- any one of the 31 nodes described in "Analog Bus Nodes"
- the A14 fractional-N VCO
- the A14 fractional-N VCO divided down to 100 kHz

The receiver portion can be the following:

- the main ADC
- the frequency counter

When analog bus traces are displayed, frequency is the x-axis. For a linear x-axis in time, switch to CW time mode (or sweep a single band).

The Main ADC

The main ADC is located on the A10 digital IF assembly and makes voltage measurements in two ranges. See "RESOLUTION", under "Analog In Menu",

The Frequency Counter

The frequency counter is located on the A14 assembly and can count one of three sources:

- selected analog bus node
- A14 fractional-N VCO (FRAC N)
- A14 fractional-N VCO divided down to 100 kHz (DIV FRAC N) (frequency range is 100 kHz to 16 MHz)

The counts are triggered by the phase lock cycle; one at each pretune, acquire, and track for each bandswitch. (The service mode, SOURCE PLL, must be ON for the counter to be updated at each bandswitch). The counter works in swept modes or in CW mode It can be used in conjunction with **[SERVICE MODES]** for troubleshooting phase lock and source problems.

To read the counter over HP-IB, use the command OUTPCNTR.

Notes

- The display and marker units (U) correspond to volts.
- Nodes 17 (1st IF) and 24 (2nd LO) are unreliable above 1 MHz.
- About 0.750 MHz is a typical counter reading with no AC signal present.
- Anything occurring during bandswitches is not visible.
- Fast-moving waveforms may be sensitive to sweep time.
- The analog bus input impedance is about 50K ohms.
- Waveforms up to approximately 200 Hz can be reproduced.

Analog In Menu

Select this menu to monitor voltage and frequency nodes, using the analog bus and internal counter, as explained below.

To switch on the analog bus and access the analog in menu, press:

(System) SERVICE MENU ANALOG BUS ON (Meas) ANALOG IN

The **[RESOLUTION [LOW]]** key toggles between low and high resolution.

Resolution	Maximum Signal	Minimum Signal
LOW	+0.5 V	−0.5 V
HIGH	+10 V	−10 V

[AUX OUT on OFF] allows you to monitor the analog bus nodes (except nodes 1, 2, 3, 4, 9, 10, 12) with external equipment (oscilloscope, voltmeter, etc.). To do this, connect the equipment to the AUX INPUT BNC connector on the rear panel, and press **[AUX OUT]**, until **[ON]** is highlighted.

Caution To prevent damage to the analyzer, first connect the signal to the rear panel AUX INPUT, and then switch the function ON.

[COUNTER: OFF] switches the internal counter off and removes the counter display from the display. The counter can be switched on with one of the next three keys. (Note: Using the counter slows the sweep.) The counter bandwidth is 16 MHz unless otherwise noted for a specific node.

Note OUTPCNTR is the HP-IB command to output the counter's frequency data.

[ANALOG BUS] switches the counter to monitor the analog bus.

[FRAC N] switches the counter to monitor the A14 fractional-N VCO frequency at the node shown on the "Overall Block Diagram," in the "Start Troubleshooting" chapter.

[DIV FRAC N] switches the counter to monitor the A14 fractional-N VCO frequency after it has been divided down to 100 kHz for phase locking the VCO.

Analog Bus Nodes

The following paragraphs describe the 31 analog bus nodes. The nodes are listed in numerical order and are grouped by assembly. Refer to the "Overall Block Diagram" for node locations.

A3 Source

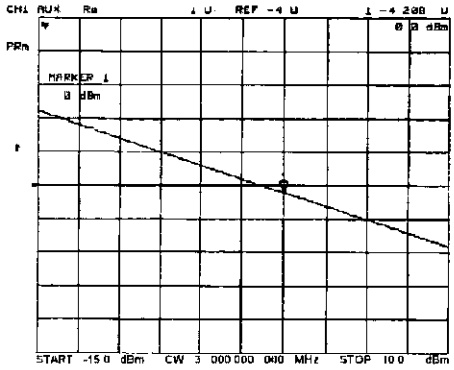
To observe six of the eight A3 analog bus nodes (not node 5 or 8), perform step A3 to set up a power sweep on the analog bus. Then follow the node specific instructions.

Step A3.
Press:
[Preset]
[System] [SERVICE MENU] [ANALOG BUS ON]
[Meas] [ANALOG IN]
[Format] [MORE] [REAL]
[Menu] [CW FREQ] [3] [G/n] [SWEEP TYPE MENU] [POWER SWEEP]
[Start] [-15] [x1]
[Stop] [10] [x1]

Node 1 **Mn Pwr DAC (main power DAC)**

Perform step A3 to set up a power sweep on the analog bus. Then press **[Meas] [ANALOG IN] [1] [x1] [Scale Ref] [AUTO SCALE].**

Node 1 is the output of the main power DAC. It sets the reference voltage to the ALC loop. At normal operation, this node should read approximately -4 volts at 0 dBm with a slope of about – 150 mV/dB. This corresponds to approximately 4 volts from -15 to + 10 dBm.



sg6262d

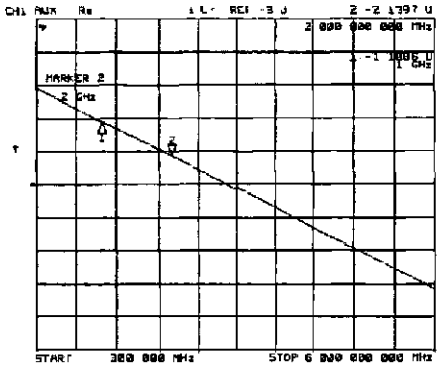
Figure 10-4. Analog Bus Node 1

Node 2 Src 1V/GHz (source 1 volt per GHz)

Press the following to view analog bus node 2:

[Preset] [Start] [3] [0] [k.m]
[System] [SERVICE MENU] [ANALOG BUS ON]
[Meas] [ANALOG IN] [2] [x1]
[Format] [MORE] [REAL]
[Scale Ref] [AUTO SCALE]

Node 2 measures the voltage on the internal voltage controlled oscillator. Or, in normal operation, it should read -1V/GHz.



sg6263d

Figure 10-5. Analog Bus Node 2

Node 3 Amp Id (amplifier current)

Press the following keys to view analog node 3:

[Preset] [System] [SERVICE MENU] [ANALOG BUS ON]
[Meas] [ANALOG IN] [3] [x1]
[Format] [MORE] [REAL]
[Scale Ref] [AUTO SCALE]

Node 3 measures the current that goes to the main IF amplifier. At normal operation this node should read about:

15 mA from 30 kHz to 299 kHz

130 mA from 300 kHz to 3 GHz

500 mA from 3 GHz to 6 GHz

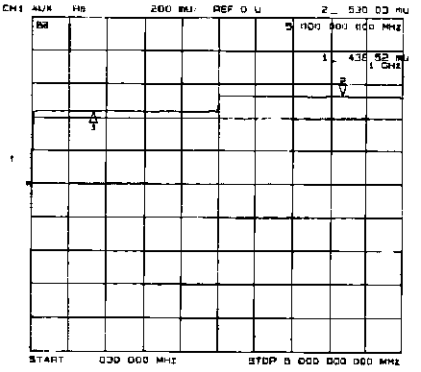


Figure 10-6. Analog Bus Node 3

Node 4 Det (detects RF OUT power level)

Perform step A3, described previously, to set up a power sweep on the analog bus. Then press **[Meas] ANALOG IN [4] [x1] [Scale Ref] [AUTO SCALE].**

Node 4 detects power that is coupled and detected from the RF OUT arm to the ALC loop. Note that the voltage exponentially follows the power level inversely. Flat segments indicate ALC saturation and should not occur between -85 dBm and + 10 dBm.

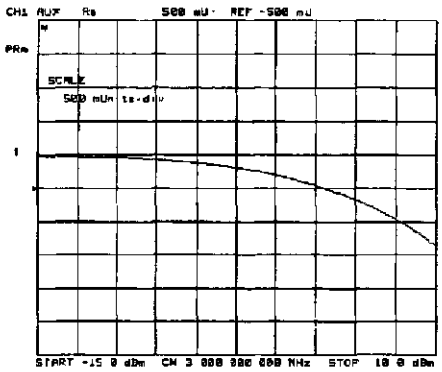


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Figure 10-7. Analog Bus Node 4

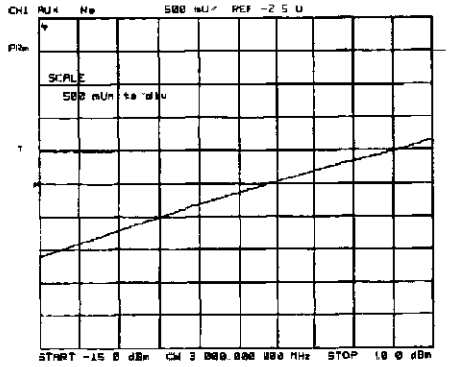
Node 5 Temp (temperature sensor)

This node registers the temperature of the cavity oscillator which must be known for effective spur avoidance. The sensitivity is 10 mV/° C. The oscillator changes frequency slightly as its temperature changes. This sensor indicates the temperature so that the frequency can be predicted.

Node 6 Integ (ALC leveling integrator output)

Perform step A3 to set up a power sweep on the analog bus. Then press **[Meas] [ANALOG IN] [6] [x1] [Scale Ref] [AUTO SCALE].**

Node 6 displays the output of the summing circuit in the ALC loop. Absolute voltage level variations are normal. When node 6 goes above 0 volts, the ALC saturation is indicated.



sg6266d

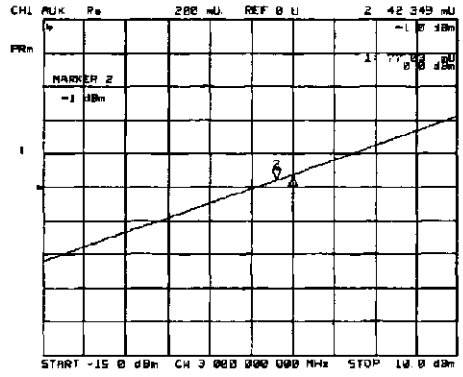
Figure 10-8. Analog Bus Node 6

Node 7 Log (log amplifier output detector)

Perform step A3 to set up a power sweep on the analog bus. Then press **[Meas] [ANALOG IN] [7] [x1] [Scale Ref] [AUTO SCALE].**

Node 7 displays the output of a logger circuit in the ALC loop. The trace should be a linear ramp with a slope of 33 mv/dB with approximately 0 volts at -3 dBm. Absolute voltage level variations are normal. Flat segments indicate ALC saturation and should not occur between -15 dBm and + 10 dBm.

The proper waveform at node 7 indicates that the circuits in the A3 source ALC loop are normal and the source is leveled.



sg6267d

Figure 10-9. Analog Bus Node 7

Node 8 A3 Gnd (ground)

A10 Digital IF

To observe the A10 analog bus nodes, perform step A10, below. Then follow the node-specific instructions.

Step A10.
Press:
[Preset]
[Meas] [ANALOG IN]
[Marker]
[System] [SERVICE MENU] [ANALOG BUS ON]
[Format] [MORE] [REAL]

Node 9 +0.37 V (+0.37 V reference)

Perform step A10, above, and then press **[Meas] [ANALOG IN] [RESOLUTION [HIGH]] [9] [x1].**

Check for a flat line at approximately +0.37 V. This is used as the voltage reference in the "Analog Bus Correction Constants" adjustment procedure. The voltage level should be the same in high and low resolution; the absolute level is not critical.

Node 10 + 2.50 V (+ 2.50 V reference)

Perform step A10, above, and then press **[Meas] [ANALOG IN] [RESOLUTION [LOW]] [10] [x1] [Scale Ref] [1] [x1].**

Check for a flat line at approximately +2.5 V. This voltage is used in the "Analog Bus Correction Constants" adjustment as a reference for calibrating the analog bus low resolution circuitry.

Node 11 Aux Input (rear panel input)

Perform step A10 and then press **[Meas] [ANALOG IN] [1] [1] [x1]**

This selects the rear panel AUX INPUT to drive the analog bus for voltage and frequency measurements. It can be used to look at test points within the instrument, using the analyzer's display as an oscilloscope. Connect the test point of interest to the rear panel AUX INPUT BNC connector.

This feature can be useful if an oscilloscope is not available. Also, it can be used for testing voltage-controlled devices by connecting the driving voltage of the device under test to the AUX IN connector. Look at the driving voltage on one display channel, while displaying the S-parameter response of the test device on the other display channel.

With **[AUX OUT]** switched ON, you can examine the analyzer' s analog bus nodes with external equipment (see **[AUX OUT on OFF]** under the "Analog Bus Menu" heading). For HP-IB considerations, see "HP-IB Service Mnemonic Definitions, " located later in this chapter.

Node 12 A10 Gnd (ground reference)

This node is used in the "Analog Bus Correction Constants" adjustment as a reference for calibrating the analog bus low and high resolution circuitry.

A11 Phase Lock

To observe the A11 analog bus nodes, perform step A11, below Then follow the node-specific instructions.

Step A11.
Press:
[Preset]
[Meas] [ANALOG IN]
[Marker]
[System] [SERVICE MENU] [ANALOG]
[Format] [MORE] [REAL]

Node 13 VCO Tune 2 (not used)

Node 14 Vbb Ref (ECL reference voltage level)

Perform step A11 and then press **[Meas] [ANALOG IN] [14] [x1] [Scale Ref] [.3] [x1] [REFERENCE VALUE] [-1.29] [x1].**

The trace should be a flat line across the entire operation frequency range within 0.3 V (one division) of the reference value. Vbb Ref is used to compensate for ECL voltage drift.

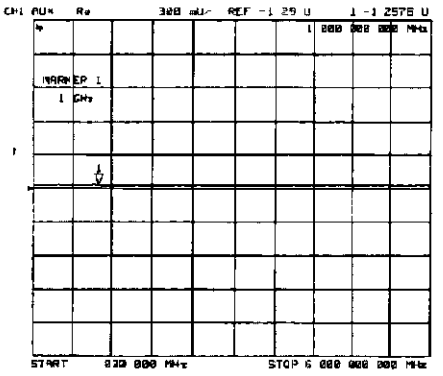


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Figure 10-10. Analog Bus Node 14

Node 15 Pretune (open-loop source pretune voltage)

Perform step All and then press **[Meas] [ANALOG IN] [15] [x1] [Scale Ref] [AUTOSCALE].**

This node displays the source pretune signal and should look like a stair-stepped ramp. Each step corresponds to the start of a band

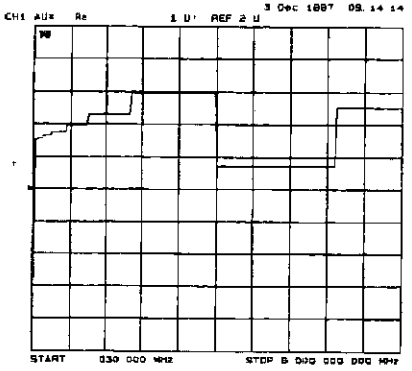
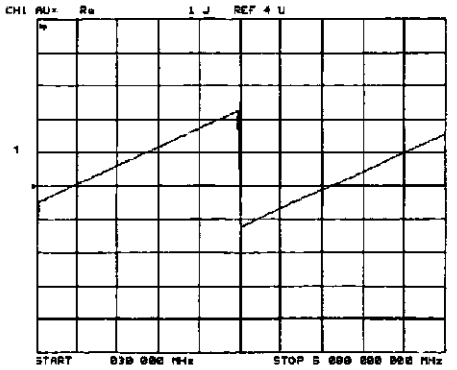


Figure 10-11. Analog Bus Node 15

Node 16 1V/GHz (source oscillator tuning voltage)

Perform step A11 and then press **[Meas] [ANALOG IN] [16] [x1] [Scale Ref] [AUTOSCALE].**

This node displays the tuning voltage ramp used to tune the source oscillator. You should see a voltage ramp like the one shown in Figure 10-12. If this waveform is correct, you can be confident that the All phase lock assembly, the A3 source assembly, the A13/A14 fractional-N assemblies, and the A7 pulse generator are working correctly and the instrument is phase locked. If you see anything else, refer to the "Source Troubleshooting" chapter.



sg6270d

Figure 10-12. Analog Bus Node 16

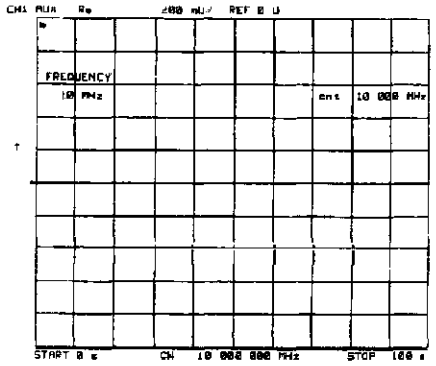
Node 17 1st IF (IF used for phase lock)

Perform step A11 and then press **[Meas] [ANALOG IN] [17] [x1] [COUNTER: ANALOG BUS] [Menu] [CW FREQ].**

Vary the frequency and compare the results to the table below.

Entered Frequency	Counter Reading
0.2 to 15.999 MHz	same as entered
16 MHz to 3 GHz	1 MHz

This node displays the IF frequency (see node17) as it enters the All phase lock assembly via the A4 R sampler assembly, This signal comes from the R sampler output and is used to phase lock the source



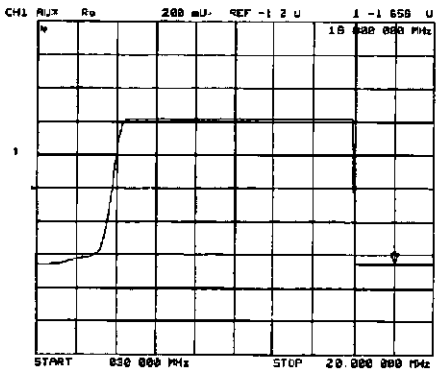
sg6271d

Figure 10-13. Counter Readout Location

Node 18 IF Det 2N (IF on A11 phase lock after 3 MHz filter)

Perform step All and then press **[Meas] [ANALOG IN] [18] [x1] [Stop] [20] [M/μ] [Scale Ref] [AUTOSCALE].**

This node detects the IF within the low pass filter/limiter. The filter is used during the track and sweep sequences but never in band 1 (3.3 to 16 MHz). The low level (about -1.7 V) means IF is in the passband of the filter. This node can be used with the FRAC N TUNE and SRC TUNE service modes.



sg6272d

Figure 10-14. Analog Bus Node 18

Node 19 IF Det 2W (IF after 16 MHz filter)

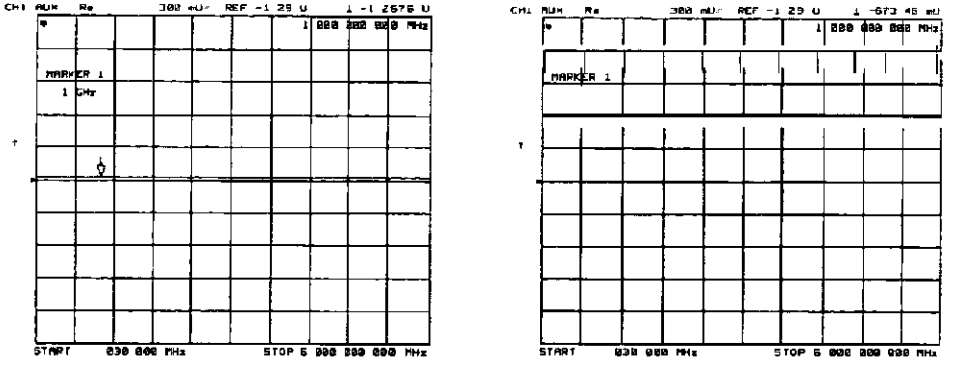
Perform step A11 and then press **[Meas] [ANALOG IN] [19] [x1] [Menu] [Stop] [20] [x1] [Scale Ref] [.2] [x1] [REFERENCE VALUE] [-1.2] [x1].**

This node detects IF after the 16 MHz filter/limiter. The filter is used during pretune and acquire, but not in band 1. Normal state is a flat line at about -1 7 v.

Node 20 IF Det 1 (IF after 30 MHz filter)

Perform step All and then press **[Meas] [ANALOG IN] [20] [x1] [Scale Ref] [0.3] [x1] [REFERENCE VALUE] [-1.29] [x1].**

The trace should be a flat line across the entire frequency band at least 0.5 V greater than Vbb (node 14). The correct trace indicates the presence of IF after the first 30 MHz filter/limiter.



sg631s

Figure 10-15. Analog Bus Node 20

A12 Reference

To observe the A12 analog bus nodes perform step A12, below. Then follow the node-specific instructions.

Step A12.
Press:
[Preset]
[Meas] [ANALOG IN]
[Marker]
[System] [SERVICE MENU] [ANALOG BUS ON]
[Format] [MORE] [REAL]

Node 21 100 kHz (100 kHz reference frequency)

Perform step Al2 and then press **[Meas] [ANALOG IN] [21] [x1] [COUNTER: ANALOG BUS].** This node counts the Al2 100 kHz reference signal that is used on Al3 (the fractional-N analog assembly) as a reference frequency for the phase detector.

Node 22 Al2 Gnd 1 (ground)

Node 23 VCO Tune (Al2 VCO tuning voltage)

Perform Step Al2 and then press **[Start] [11] [M/μ] [STOP] [21] [M/μ] [Meas] [ANALOG IN] [23] [x1] [Marker] [Scale Ref] [AUTO SCALE].**

The trace should show a voltage step as shown in Figure 10-16. At normal operation, the left half trace should be 0 ±1000 mV and the right half trace should be 100 to 200 mV higher (that is, one to two divisions). If the trace does not appear as shown in Figure 10-16, refer to the "High/Low Band Transition Adjustment" in the "Adjustments and Correction Constants" chapter.

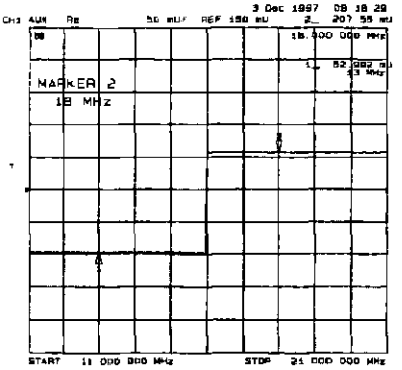


Figure 10-16. Analog Bus Node 23

Node 24 2nd LO

Perform step A12 and then press **[Meas] [ANALOG IN] [24] [x1] [COUNTER: ANALOG BUS] [Menu] [CW FREQ].**

This node counts the 2nd LO used by the sampler/mixer assemblies to produce the 2nd IF of 4 kHz. As you vary the frequency, the counter reading should change to values very close to those indicated below:

Frequency Entered	Counter Reading
0.03 to 1 MHz	frequency entered +4 kHz
1 to 16 MHz	not accurate
16 to 3,000 MHz	996 kHz

Node 25 PL Ref (phase lock reference)

Perform step A12 and then press **[Meas] [ANALOG IN] [25] [x1] [COUNTER: ANALOG BUS] [Menu] [CW FREQ].**

This node counts the reference signal used by the phase comparator circuit on the A11 phase lock assembly. As you vary the frequency, the counter reading should change as indicated below:

Frequency Entered	Counter Reading
0.3 to 1 MHz	frequency entered
1 to 16 MHz	not accurate
16 to 3,000 MHz	1 MHz

Node 26 Ext Ref (rear panel external reference input)

Perform step A12 and then press **[Meas] [ANALOG IN] [26] [x1]**

The voltage level of this node indicates whether an external reference timebase is being used:

- No external reference: about -0.9 V
- With external reference: about -0.6 V.

Node 27 VCXO Tune (40 MHz VCXO tuning voltage)

Perform step A12 and then press **[Meas] [ANALOG IN] [27] [x1] [Marker Fctn]. [MARKER —>REFERENCE].**

This node displays the voltage used to fine tune the A12 reference VCXO to 40 MHz. You should see a flat line at some voltage level (the actual voltage level varies from instrument to instrument). Anything other than a flat line indicates that the VCXO is tuning to different frequencies. Refer to the "Frequency Accuracy" adjustment procedure.

Node 28 A12 Gnd 2 (Ground reference)

A14 Fractional-N (Digital)

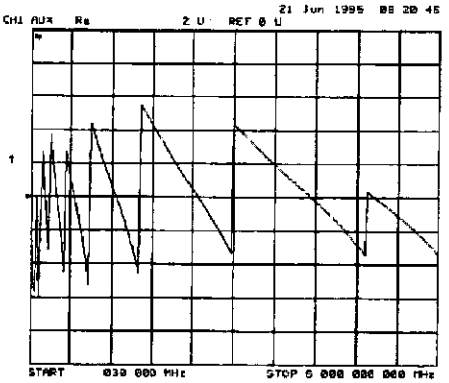
To observe the A14 analog bus nodes perform step A14, below. Then follow the node-specific instructions.

Step A14.
Press:
[Preset]
[Meas] [ANALOG IN]
[System] [SERVICE MENU] [ANALOG BUS ON]
[Format] [MORE] [REAL]

Node 29 FN VCO Tun (A14 FN VCO tuning voltage)

Perform step A14 and then press **[Meas] [ANALOG IN] [29] [x1] [Scale Ref] [AUTOSCALE].**

Observe the A14 FN VCO tuning voltage. If the A13 and A14 assemblies are functioning correctly and the VCO is phase locked, the trace should look like Figure 10-17. Any other waveform indicates that the FN VCO is not phase locked. The vertical lines in the trace indicate the band crossings. (The counter can also be enabled to count the VCO frequency in CW mode.)



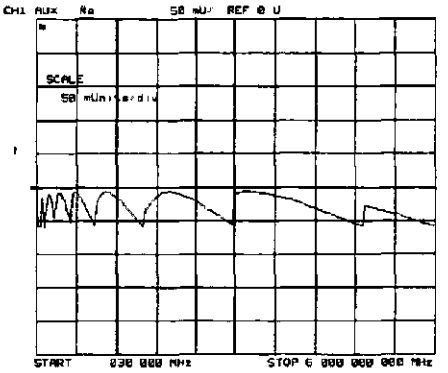
sg6274d

Figure 10-17. Analog Bus Node 29

Node 30 FN VCO Det (A14 VCO detector)

Perform step A14 and then press **[Meas] [ANALOG IN] [30] [x1] [RESOLUTION [HIGH]] [Scale Ref] [50] [k/m].**

See whether the FN VCO is oscillating. The trace should resemble Figure 10-18.



sg6275d

Figure 10-18. Analog Bus Node 30

Node 31 Count Gate (analog bus counter gate)

Perform step A14 and then press **[Meas] [ANALOG IN] [31] [x1] [Scale Ref] [2] [x1].**

You should see a flat line at +5 V across the operating frequency range. The counter gate activity occurs during bandswitches, and therefore is not visible on the analog bus. To view the bandswitch activity, look at this node on an oscilloscope, using **[AUX OUT ON]** Refer to **[AUX OUT on OFF]** under the Analog Bus Menu heading.

PEEK/POKE Menu

To access this menu, press **[System] [SERVICE MENU] [PEEK/POKE].**

[PEEK/POKE]	allows you to edit the content of one or more memory addresses. The keys are described below.

Caution The PEEK/POKE capability is intended for service use only.

[PEEK/POKE ADDRESS] (PEEL[D])	accesses any memory address and shows it in the active entry area of the display. Use the front panel knob, entry keys, or step keys to enter the memory address of interest
[PEEK] (PEEK)	displays the data at the accessed memory address.
[POKE] (POKE[D])	allows you to change the data at the memory address accessed by the **[PEEK/POKE ADDRESS]** softkey. Use the front panel knob, entry keys, or step keys to change the data. The A9CC switch must be in the "ALTER" position in order to poke.
[RESET MEMORY]	resets or clears the memory where instrument states are stored. lb do this, press **[RESET MEMORY] [Preset].**

Firmware Revision Softkey

Press **[System] [SERVICE MENU] [FIRMWARE REVISION]** to display the current firmware revision information. The number and implementation date appear in the active entry area of the display as shown in Figure 10-19 below. The analyzer's serial number and installed options are also displayed. Another way to display the firmware revision information is to cycle the line power.

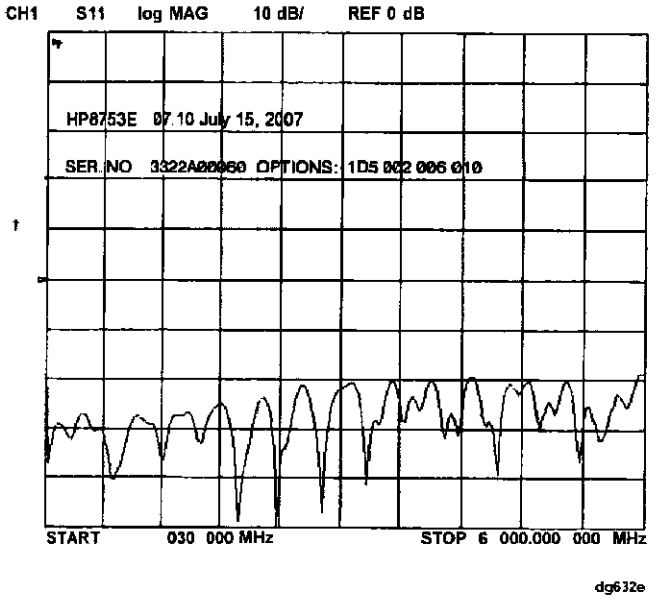


Figure 10-19. Location of Firmware Revision Information on Display

HP-IB Service Mnemonic Definitions

All service routine keystrokes can be made through HP-IB in one of the following approaches:

- sending equivalent remote HP-IB commands. (Mnemonics have been documented previously with the corresponding keystroke.)
- invoking the System Menu (MENUSYST) and using the analyzer mnemonic (SOFTn), where "n" represents the softkey number. (Softkeys are numbered 1 to 8 from top to bottom.)

An HP-IB overview is provided in the "Compatible Peripherals" chapter in the *User's Guide*. HP-IB programming information is also provided in the Programming Guide.

Invoking Tests Remotely

Many tests require a response to the displayed prompts. Since bit 1 of the Event Status Register B is set (bit 1 = service routine waiting) any time a service routine prompts the user for an expected response, you can send an appropriate response using one of the following techniques:

- Read event status register B to reset the bit.
- Enable bit 1 to interrupt (ESNB[D]). See "Status Reporting" in the *Programming Guide*.
- Respond to the prompt with a TESRn command (see Tests Menu, at the beginning of this chapter).

Symbol Conventions

[ ]	An optional operand
D	A numerical operand
< >	A necessary appendage
|	An either/or choice in appendages

Analog Bus Codes

ANAI[D]	Measures and displays the analog input. The preset state input to the analog bus is the rear panel AUX IN. The other 30 nodes may be selected with **[D]** only if the ABUS is enabled (ANABon)
OUTPCNTR	Outputs the counter's frequency data.
OUTPERRO	Reads any prompt message sent to the error queue by a service routine.
OUTPTESS	Outputs the integer status of the test most recently executed. Status codes are those listed under "TST?".
TST?	Executes the power-on self test (internal test 1) and outputs an integer test status. Status codes are as follows: 0 = pass 1 = fail 2 = in progress 3 = not available 4 = not done 5 = done

Error Messages

This section contains an alphabetical list of the error messages that pertain to servicing the analyzer. The information in the list includes explanations of the displayed messages and suggestion to help solve the problem.

Note The error messages that pertain to measurement applications are included in the *HP 8753E Network Analyzer User's Guide*.

BATTERY FAILED. STATE MEMORY CLEARED

Error Number 183 The battery protection of the non-volatile SRAM memory has failed. The SRAM memory has been cleared. Refer to the "Assembly Replacement and Post-Repair Procedures" chapter for battery replacement instructions. See the "Preset State and Memory Allocation, " chapter in the *HP 8753E Network Analyzer User's Guide* for more information about the SRAM memory.

BATTERY LOW! STORE SAVE REGS TO DISK

Error Number 184 The battery protection of the non-volatile SRAM memory is in danger of failing. If this occurs, all of the instrument state registers stored in SRAM memory will be lost. Save these states to a disk and refer to the "Assembly Replacement and Post-Repair Procedures" chapter for battery replacement instructions. See the "Preset State and Memory Allocation." chapter in the *HP 8753E Network Analyzer User's Guide* for more information about the SRAM memory.

CALIBRATION ABORTED

Error Number 74 You have changed the active channel during a calibration so the calibration in progress was terminated. Make sure the appropriate channel is active and restart the calibration.

CALIBRATION REQUIRED

Error Number 63 — A calibration set could not be found that matched the current stimulus state or measurement parameter. You will have to perform a new calibration.

CORRECTION CONSTANTS NOT STORED

Error Number 3 — A store operation to the EEPROM was not successful. You must change the position of the jumper on the A9 CPU assembly. Refer to the "A9 CC Jumper Position Procedure" in the "Adjustments and Correction Constants" chapter.

CORRECTION TURNED OFF

Error Number 66 — Critical parameters in your current instrument state do not match the parameters for the calibration set, therefore correction has been turned off. The critical instrument state parameters are sweep type, start frequency, frequency span, and number of points.

CURRENT PARAMETER NOT IN CAL SET

Error Number 64 — Correction is not valid for your selected measurement parameter. Either change the measurement parameters or perform a new calibration.

DEADLOCK

Error Number 111 — A fatal firmware error occurred before instrument preset completed.

DEVICE: not on, not connect, wrong addrs

Error Number 119 — The device at the selected address cannot be accessed by the analyzer. Verify that the device is switched on, and check the HP-IB connection between the analyzer and the device. Ensure that the device address recognized by the analyzer matches the HP-IB address set on the device itself.

DISK HARDWARE PROBLEM

Error Number 39 — The disk drive is not responding correctly. Refer to the disk drive operating manual.

DISK MESSAGE LENGTH ERROR

Error Number 190 — The analyzer and the external disk drive aren't communicating properly. Check the HP-IB connection and then try substituting another disk drive to isolate the problem instrument.

DISK: not on, not connected, wrong addrs

Error Number 38 — The disk cannot be accessed by the analyzer. Verify power to the disk drive, and check the HP-IB connection between the analyzer and the disk drive. Ensure that the disk drive address recognized by the analyzer matches the HP-IB address set on the disk drive itself.

DISK READ/WRITE ERROR

Error Number 189: There may be a problem with your disk. Try a new floppy disk. If a new floppy disk does not eliminate the error, suspect hardware problems.

INITIALIZATION FAILED

Error Number 47: The disk initialization failed, probably because the disk is damaged.

INSUFFICIENT MEMORY, PWR MTR CAL OFF

Error Number 154: There is not enough memory space for the power meter calibration array. Increase the available memory by clearing one or more save/recall registers, or by reducing the number of points.

NO CALIBRATION CURRENTLY IN PROGRESS

Error Number 69: The **[RESUME CAL SEQUENCE]** softkey is not valid unless a calibration is already in progress. Start a new calibration.

NOT ENOUGH SPACE ON DISK FOR STORE

Error Number 44: The store operation will overflow the available disk space. Insert a new disk or purge files to create free disk space.

NO FILE(S) FOUND ON DISK

Error Number 45 — No files of the type created by an analyzer store operation were found on the disk. If you requested a specific file title, that file was not found on the disk.

NO IF FOUND: CHECK R INPUT LEVEL

Error Number 5 — The first IF signal was not detected during pretune. Check the front panel R channel jumper. If there is no visible problem with the jumper, refer to the "Source Troubleshooting" chapter.

NO PHASE LOCK: CHECK R INPUT LEVEL

Error Number 7 — The first IF signal was detected at pretune, but phase lock could not be acquired. Refer to the "Source Troubleshooting" chapter.

NO SPACE FOR NEW CAL. CLEAR REGISTERS

Error Number 70 — You cannot store a calibration set due to insufficient memory. You can free more memory by clearing a saved instrument state from an internal register (which may also delete an associated calibration set, if all the instrument states using the calibration kit have been deleted.) You can store the saved instrument state and calibration set to a disk before clearing them. After deleting the instrument states, press **[Preset]** to run the memory packer

NOT ALLOWED DURING POWER METER CAL

Error Number 198: When the analyzer is performing a power meter calibration, the HP-IB bus is unavailable for other functions such as printing or plotting.

OVERLOAD ON INPUT A, POWER REDUCED

Error Number 58: See error number 57.

OVERLOAD ON INPUT B, POWER REDUCED

Error Number 59: See error number 57.

OVERLOAD ON INPUT R, POWER REDUCED

Error Number 57: You have exceeded approximately + 14 dBm at one of the test ports. The RF output power is automatically reduced to -85 dBm. The annotation P⇓ appears in the left margin of the display to indicate that the power trip function has been activated. When this occurs, reset the power to a lower level, then toggle the **[SOURCE PWR on OFF]** softkey to switch on the power again.

PARALLEL PORT NOT AVAILABLE FOR GPIO

Error Number 165: You have defined the parallel port as COPY for sequencing in the HP-IB menu. To access the parallel port for general purpose I/O (GPIO), set the selection to [GPIO].

PARALLEL PORT NOT AVAILABLE FOR COPY

Error Number 167: You have defined the parallel port as general purpose I/O (GPIO) for sequencing. The definition was made under the **[Local]** key menus. To access the parallel port for copy, set the selection to **[PARALLEL [COPY]]**.

PHASE LOCK CAL FAILED

Error Number 4: An internal phase lock calibration routine is automatically executed at power-on, preset, and any time a loss of phase lock is detected. This message indicates that phase lock calibration was initiated and the first IF detected, but a problem prevented the calibration from completing successfully. Refer to Chapter 3, "Adjustments and Correction Constants" and execute pretune correction (test 48).

This message may appear if you connect a mixer between the RF output and R input before turning on frequency offset mode. Ignore it: it will go away when you turn on frequency offset. This message may also appear if you turn on frequency offset mode before you define the offset.

PHASE LOCK LOST

Error Number 8: Phase lock was acquired but then lost. Refer to the "Source Troubleshooting" chapter.

POSSIBLE FALSE LOCK

Error Number 6: Phase lock has been achieved, but the source may be phase locked to the wrong harmonic of the synthesizer. Perform the source pretune correction routine documented in the "Adjustments and Correction Constants" chapter.

POWER METER INVALID

Error Number 116: The power meter indicates an out-of-range condition. Check the test setup.

POWER METER NOT SETTLED

Error Number 118: Sequential power meter readings are not consistent. Verify that the equipment is set up correctly. If so, preset the instrument and restart the operation.

POWER SUPPLY HOT!

Error Number 21: The temperature sensors on the A8 post-regulator assembly have detected an over-temperature condition. The power supplies regulated on the post-regulator have been shut down. Refer to the "Power Supply Troubleshooting" chapter.

POWER SUPPLY SHUT DOWN!

Error Number 22: One or more supplies on the A8 post-regulator assembly have been shut down due to an over-current, over-voltage, or under-voltage condition. Refer to the "Power Supply Troubleshooting" chapter.

POWER UNLEVELED

Error Number 179 — There is either a hardware failure in the source or you have attempted to set the power level too high. Check to see if the power level you set is within specifications. If it is, refer to the "Source Troubleshooting" chapter. You will only receive this message over the HP-IB. On the analyzer, P? is displayed.

PRINTER: error

Error Number 175 — The parallel port printer is malfunctioning. The analyzer cannot complete the copy function.

PRINTER: not handshaking

Error Number 177 — The printer at the parallel port is not responding.

PRINTER: not on, not connected, wrong addrs

Error Number 24 — The printer does not respond to control. Verify power to the printer, and check the HP-IB connection between the analyzer and the printer. Ensure that the printer address recognized by the analyzer matches the HP-IB address set on the printer itself.

PROBE POWER SHUT DOWN!

Error Number 23 — The analyzer biasing supplies to the HP 85024A external probe are shut down due to excessive current Troubleshoot the probe, and refer to the "Power Supply Troubleshooting" chapter.

PWR MTR: NOT ON/CONNECTED OR WRONG ADDRS

Error Number 117 — The power meter cannot be accessed by the analyzer. Verify that the power meter address and model number set in the analyzer match the address and model number of the actual power meter.

SAVE FAILED. INSUFFICIENT MEMORY

Error Number 151 — You cannot store an instrument state in an internal register due to insufficient memory. Increase the available memory by clearing one or more save/recall registers and pressing **[Preset]** or by storing files to a disk.

SELF TEST #n FAILED

Service Error Number 112 — Internal test #n has failed Several internal test routines are executed at instrument preset. The analyzer reports the first failure detected. Refer to the internal tests and the self-diagnose feature descriptions earlier in this chapter.

SOURCE POWER TURNED OFF, RESET UNDER POWER MENU

Information Message — You have exceeded the maximum power level at one of the inputs and power has been automatically reduced. The annotation P⇓ indicates that power trip has been activated. When this occurs, reset the power and then press **[Menu] [POWER] [SOURCE PWR on OFF]**, to switch on the power. This message follows error numbers 57, 58, and 59.

SWEEP MODE CHANGED TO CW TIME SWEEP

Error Number 187 — If you select external source auto or manualinstrumentmode and you do not also select CW mode, the analyzer is automatically switched to CW.

TEST ABORTED

Error Number 113 — You have prematurely stopped a service test.

TROUBLE! CHECK SETUP AND START OVER

Service Error Number 115 — Your equipment setup for the adjustment procedure in progress is not correct. Check the setup diagram and instructions in the "Adjustments and Correction Constants" chapter. Start the procedure again.

WRONG DISK FORMAT, INITIALIZE DISK

Error Number 77 — You have attempted to store, load, or read file titles, but your disk format does not conform to the Logical Interchange Format (LIF). You must initialize the disk before reading or writing to it.

11

Error Terms

The analyzer generates and stores factors in internal arrays when a measurement error-correction (measurement calibration) is performed. These factors are known by the following terms:

- error terms
- E-terms
- measurement calibration coefficients

The analyzer creates error terms by measuring well-defined calibration devices over the frequency range of interest and comparing the measured data with the ideal model for the devices. The differences represent systematic (repeatable) errors of the analyzer system. The resulting calibration coefficients are good representations of the systematic error sources For details on the various levels of error-correction, refer to the "Optimizing Measurement Results" chapter of the *HP 8753E Network Analyzer User's Guide* For details on the theory of error-correction, refer to the "Application and Operation Concepts" chapter of the *HP 8753E Network Analyzer User's Guide*.

Error Terms Can Also Serve a Diagnostic Purpose

Specific parts of the analyzer and its accessories directly contribute to the magnitude and shape of the error terms. Since we know this correlation and we know what typical error terms look like, we can examine error terms to monitor system performance (preventive maintenance) or to identify faulty components in the system (troubleshooting).

- **Preventive Maintenance:** A stable, repeatable system should generate repeatable error terms over long time intervals, for example, six months. If you make a hardcopy record (print or plot) of the error terms, you can periodically compare current error terms with the record. A sudden shift in error terms reflects a sudden shift in systematic errors, and may indicate the need for further troubleshooting. A long-term trend often reflects drift,

connector and cable wear, or gradual degradation, indicating the need for further investigation and preventive maintenance. Yet, the system may still conform to specifications. The cure is often as simple as cleaning and gaging connectors or inspecting cables.

- **Troubleshooting:** If a subtle failure or mild performance problem is suspected, the magnitude of the error terms should be compared against values generated previously with the same instrument and calibration kit. This comparison will produce the most precise view of the problem.

  However, if previously generated values are not available, compare the current values to the typical values listed in Table 11-2, and shown graphically on the plots in this chapter. If the magnitude exceeds its limit, inspect the corresponding system component. If the condition causes system verification to fail, replace the component.

  Consider the following while troubleshooting:

  - All parts of the system, including cables and calibration devices, can contribute to systematic errors and impact the error terms.
  - Connectors must be clean, gaged, and within specification for error term analysis to be meaningful.
  - Avoid unnecessary bending and flexing of the cables following measurement calibration, minimizing cable instability errors.
  - Use good connection techniques during the measurement calibration" The connector interface must be repeatable. Refer to the "Principles of Microwave Connector Care" section in the "Service Equipment and Analyzer Options" chapter for information on connection techniques and on cleaning and gaging connectors.
  - Use error term analysis to troubleshoot minor, subtle performance problems. Refer to the "Start Troubleshooting Here" chapter if a blatant failure or gross measurement error is evident.
  - It is often worthwhile to perform the procedure twice (using two distinct measurement calibrations) to establish the degree of repeatability If the results do not seem repeatable, check all connectors and cables.

Full Two-Port Error-Correction Procedure

Note This is the most accurate error-correction procedure. Since the analyzer takes both forward and reverse sweeps, this procedure takes more time than the other correction procedures.

1. Set any measurement parameters that you want for the device measurement: power, format, number of points, IF bandwidth.
2. To access the measurement correction menus, press:

   [Cal]
3. If your calibration kit is different than the kit specified under the **[CAL KIT [ ]]** softkey, press:

   [CAL KIT] [SELECT CAL KIT] (select your type of kit)

   [RETURN]
4. To select the correction type, press:

   [CALIBRATE MENU] [FULL 2-PORT] [REFLECTION]
5. Connect a shielded open circuit to PORT 1.

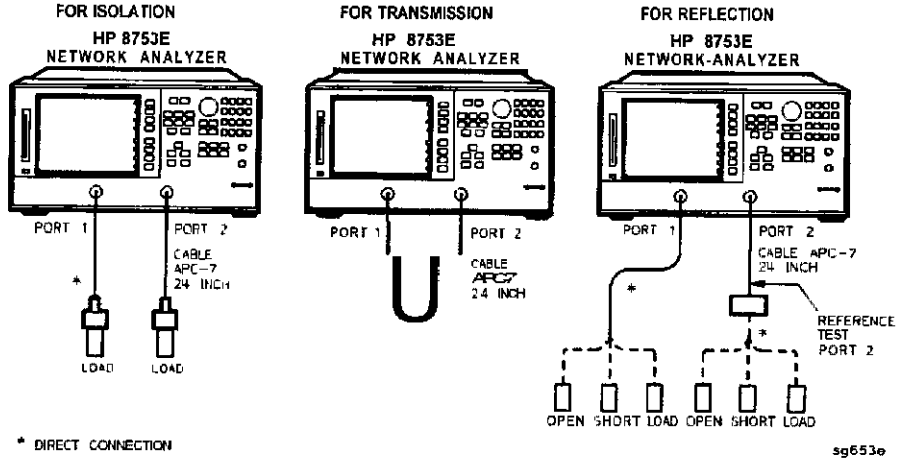


Figure 11-1. Standard Connections for Full Two-Port Error-Correction

6. To measure the standard, when the displayed trace has settled, press:

   [FORWARD: OPEN]

   The analyzer underlines the **[OPEN]** softkey after it measures the standard.

7. Disconnect the open, and connect a short circuit to PORT 1.
8. To measure the device, when the displayed trace has settled, press:

   [FORWARD: SHORT]

   The analyzer underlines the **[SHORT]** softkey after it measures the standard.

9. Disconnect the short, and connect an impedance-matched load to PORT 1.
10. To measure the standard, when the displayed trace has settled, press:

    [FORWARD: LOAD]

    The analyzer underlines the **[LOAD]** softkey after it measures the standard

11. Repeat the open-short-load measurements descried above, but connect the devices in turn to PORT 2, and use the **[REVERSE: OPEN]**, **[REVERSE: SHORT]**, and **[REVERSE: LOAD]** softkeys
12. To compute the reflection correction coefficients, press:

    [STANDARDS DONE]

13 To start the transmission portion of the correction, press: **[TRANSMISSION]**.

14. Make a "through" connection between the points where you will connect your device under test as shown in Figure 11-1.

Note Include any adapters or cables that you will have in the device measurement. That is, connect the standard device where you will connect your device under test.

Note The through in most calibration kits is defined with zero length. The correction will not work properly if a non-zero length through is used, unless the calibration kit is modified to change the defined through to the length used. This is important for measurements of non-insertable devices (devices having ports that are both male or both female). The modified calibration kit must be saved as the user calibration kit, and the **[USER KIT]** must be selected before the calibration is started.

15. To measure the standard, when the trace has settled, press:

    [DO BOTH FWD+REV]

    The analyzer underlines the softkey label after it makes each measurement.

16. Press **[ISOLATION]** and select from the following two options:

    - If you will be measuring devices with a dynamic range less than 90 dB, press:

      [OMIT ISOLATION] [ISOLATION DONE].

    - If you will be measuring devices with a dynamic range greater than 90 dB, follow these steps:

      a. Connect impedance-matched loads to PORT 1 and PORT 2.

Note If you will be measuring highly reflective devices, such as filters, use the test device, connected to the reference plane and terminated with a load, for the isolation standard.

      b. Activate at least four times more averages than desired during the device measurement.

      c. Press **[Cal] [RESUME CAL SEQUENCE] [FWD ISOL'N ISOL'N STD] [REV ISOL'N ISOL'N STD] [ISOLATION DONE].**

      d. Return the averaging to the original state of the measurement, and press **[Cal] [RESUME CAL] [SEQUENCE]** .

17. To compute the error coefficients, press:

    [DONE 2-PORT CAL]

The analyzer displays the corrected measurement trace. The analyzer also shows the notation Cor at the left of the screen, indicating that error-correction is on.

Note You can save or store the measurement correction to use for later measurements. Use the menus under **[Save/Recall]**, or refer to "Printing, Plotting, and Saving Measurement Results" located in the *HP 8753E Network Analyzer User's Guide* for procedures.

18. This completes the full two-port correction procedure. You can connect and measure your device under test.

Table 11-1. Calibration Coefficient Terms and Tests

Calibration Coefficient	Calibration Type				Test Number
	Response	Response and Isolation*	1-port	2-port†	
1	E_R or E_T	E_X (E_D)	E_D	E_{DF}	32
2		E_T (E_R)	E_S	E_{SF}	33
3			E_R	E_{RF}	34
4				E_{XF}	35
5				E_{LF}	36
6				E_{TF}	37
7				E_{DR}	38
8				E_{SR}	39
9				E_{RR}	40
10				E_{XR}	41
11				E_{LR}	42
12				E_{TR}	43

NOTES:

Meaning of first subscript: D-directivity; S-source match; R-reflection tracking; X=crosstalk, L=load match; T= transmission tracking.

Meaning of second subscript F=forward; R-reverse.

* Response and Isolation cal yields: E_X or E_T if a transmission parameter (S_{21}, S_{12}) or E_D or E_R if a reflection parameter (S_{11}, S_{22}).

† One-path, 2-port cal duplicates arrays 1 to 6 in arrays 7 to 12

Error Term Inspection

Note If the correction is not active, press **[Cal] [CORRECTION ON].**

1. Press **[System] [SERVICE MENU] [TESTS] [32] [xl] [EXECUTE TEST].**

   The analyzer copies the first calibration measurement trace for the selected error term into memory and then displays it. Table 11-2 lists the test numbers.

2. Press **[Scale Ref]** and adjust the scale and reference to study the error term trace.

3. Press **[Marker Fctn]** and use the marker functions to determine the error term magnitude.

4. Compare the displayed measurement trace to the trace shown in the following "Error Term descriptions" section, and to previously measured data. If data is not available from previous measurements, refer to the typical uncorrected performance specifications listed in Table 11-2.

5. Make a hardcopy of the measurement results.

   a. Connect a printing or plotting peripheral to the analyzer.

   b. Press **[Local] [SYSTEM CONTROLLER] [SET ADDRESSES]** and select the appropriate peripheral to verify that the HP-IB address is set correctly on the analyzer.

   c. Press **[Save/Recall]** and then choose either **[PRINT]** or **[PLOT].**

   d. Press **[Display] [MORE] [TITLE]** and title each data trace so that you can identify it later.

   For detailed information on creating hardcopies, refer to "Printing, Plotting, and Saving Measurement Results" in the *HP 8753E Network Analyzer User's Guide*

If Error Terms Seem Worse than Typical Values

1. Perform a system verification to verify that the system still conforms to specifications.
2. If system verification fails, refer to "Start Troubleshooting Here."

Uncorrected Performance

The following table shows typical performance without error-correction. RF cables are not used except as noted. Related error terms should be within these values.

Table 11-2. Uncorrected System Performance

	Frequency Range (GHz)	
	0.0003 to 3.0	3.0 to 6.0
Directivity	30 dB	25 dB
Source Match	16 dB	14 dB
Load Match	16 dB	14 dB
Reflection Tracking*	±1.5 dB	+ 0.5 dB, -2.6 dB
Transmission Tracking*	±1.5 dB	+ 0.5 dB, -2.5 dB
Crosstalk	90 dB	80 dB

* Deviation from nominal trace across the frequency range.

Error Term Descriptions

The error term descriptions in this section include the following information:

- significance of each error term
- typical results following a full 2-port error-correction
- guidelines to interpret each error term

The same description applies to both the forward (F) and reverse (R) terms

Directivity (EDF and EDR)

Description

Directivity is a measure of any detected power that is reflected when a load is attached to the test port These are the uncorrected forward and reverse directivity error terms of the system. The directivity error of the test port is determined by measuring the reflection (S11, S22) of the load during the error-correction procedure

Significant System Components

- load used in the error-correction (calibration)
- test port connectors
- test port cables

Affected Measurements

Low reflection device measurements are most affected by directivity errors.

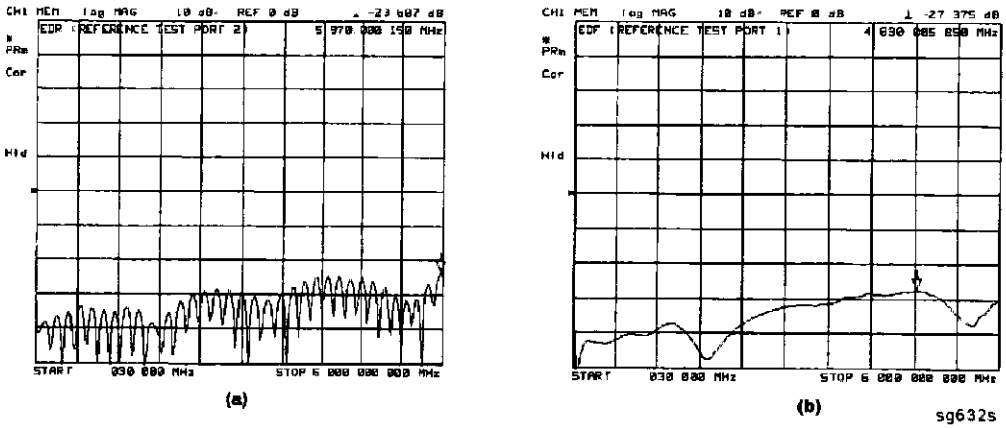


Figure 11-2. Typical EDF/EDR without and with Cables

Source Match (ESF and ESR)

Description

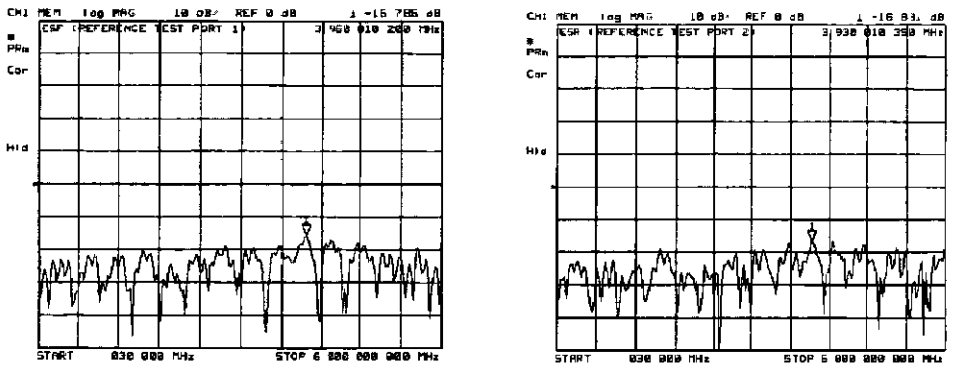
Source match is a measure of test port connector match, as well as the match between all components from the source to the test port. These are the forward and reverse uncorrected source match terms of the driven port.

Significant System Components

- load calibration kit device
- open calibration kit device
- short calibration kit device
- bridge
- test port connectors
- bias tees
- step attenuator
- transfer switch
- test port cables

Affected Measurements

Reflection and transmission measurements of highly reflective devices are most affected by source match errors



sg633s

Figure 11-3. Typical ESF/ESR without and with Cables

Reflection Tracking (ERF and ERR)

Description

Reflectian tracking is the difference between the frequency response of the reference path (R path) and the frequency response of the reflection test path (A or B input path).

Significant System Components

- open calibration kit device
- short calibration kit device
- R signal path if large variation in both ERF and ERR
- A or B input paths if only one term is affected

Affected Measurements

All reflection measurements (high or low return loss) are affected by the reflection tracking errors.

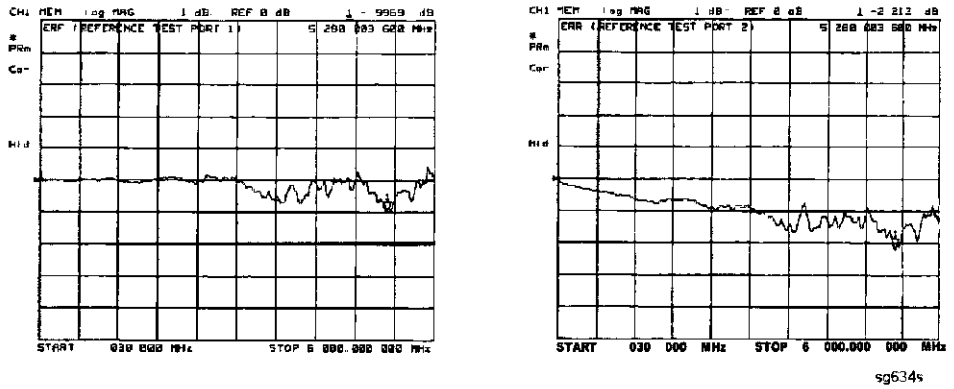


Figure 11-4. Typical ERF/ERR without and with Cables

Isolation (Crosstalk, EXF and EXR)

Description

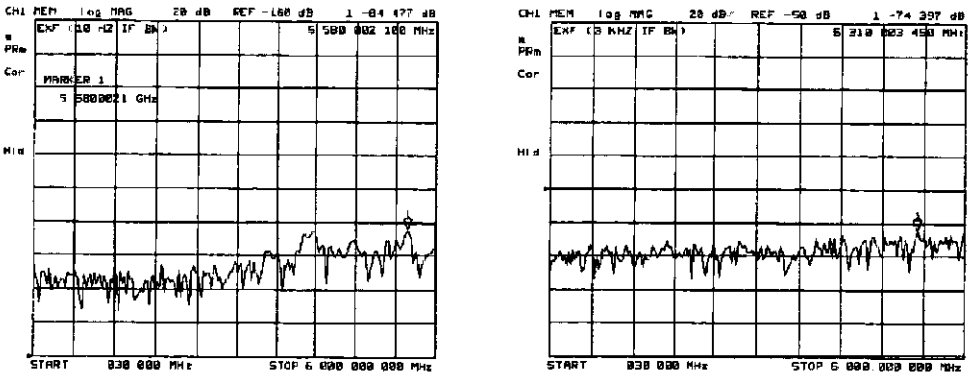
Isolation is a measure of the leakage between the test ports and the signal paths. The isolation error terms are characterized by measuring transmission (S21, S12) with loads attached to both ports during the error-correction procedure. Since these terms are low in magnitude, they are usually noisy (not very repeatable). The error term magnitude changes dramatically with IF bandwidth: a 10 Hz IF bandwidth must be used in order to lower the noise floor beyond the crosstalk specification. Using averaging will also reduce the peak-to-peak noise in this error term.

Significant System Components

- sampler crosstalk

Affected Measurements

Transmission measurements, (primarily where the measured signal level is very low), are affected by isolation errors. For example, transmission measurements where the insertion loss of the device under test is large.



sg638s

Figure 11-5.
Typical EXF/EXR with 10 Hz Bandwidth and with 3 kHz Bandwidth

Load Match (ELF and ELR)

Description

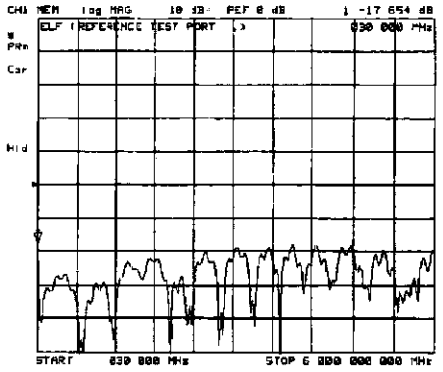
Load match is a measure of the impedance match of the test port that terminates the output of a Z-port device. Load match error terms are characterized by measuring the reflection (S11, S22) responses of a "through" configuration during the calibration procedure.

Significant System Components

- "through" cable
- cable connectors
- test port connectors

Affected Measurements

All transmission and reflection measurements of a low insertion loss two-port devices are most affected by load match errors. Transmission measurements of lossy devices are also affected.



sg6277d

Figure 11-6. Typical ELF/ELR

Transmission Tracking (ETF and ETR)

Description

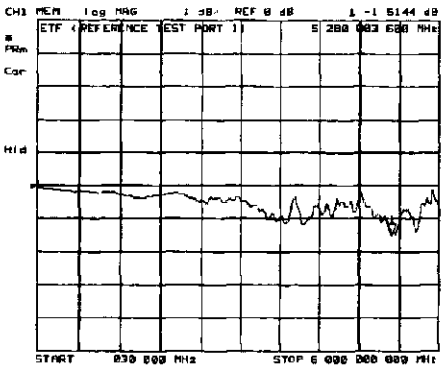
Transmission tracking is the difference between the frequency response of the reference path (including R input) and the transmission test path (including A or B input) while measuring transmission. The response of the test port cables is included. These terms are characterized by measuring the transmission (S21, S12) of the "through" configuration during the error-correction procedure.

Significant System Components

- R signal path (if both ETF and ETR are bad)
- A or B input paths
- "through" cable

Affected Measurements

All transmission measurements are affected by transmission tracking errors.



sg6278d

Figure 11-7. Typical ELF/ELR

12

Theory of Operation

This chapter is divided into two major sections:

- "How the HP 8753E Works" gives a general description of the HP 8753E network analyzer operation.
- "A Close Look at the Analyzer's Functional Groups" provides more detailed operating theory for each of the analyzer's functional groups.

How the HP 8753E Works

Network analyzers measure the reflection and transmission characteristics of devices and networks. A network analyzer test system consists of the following:

- source
- signal-separation devices
- receiver
- display

The analyzer applies a signal that is either transmitted through the device under test, or reflected from its input, and then compares it with the incident signal generated by the swept RF source. The signals are then applied to a receiver for measurement, signal processing, and display.

The HP 8753E vector network analyzer integrates a high resolution synthesized RF source, test set, and a dual channel three-input receiver to measure and display magnitude, phase, and group delay of transmitted and reflected power. The HP 8753E Option 010 has the additional capability of transforming measured data from the frequency domain to the time domain. Figure 12-1 is a simplified block diagram of the network analyzer system. A detailed block diagram of the analyzer is located at the end of Chapter 4, "Start Troubleshooting Here."

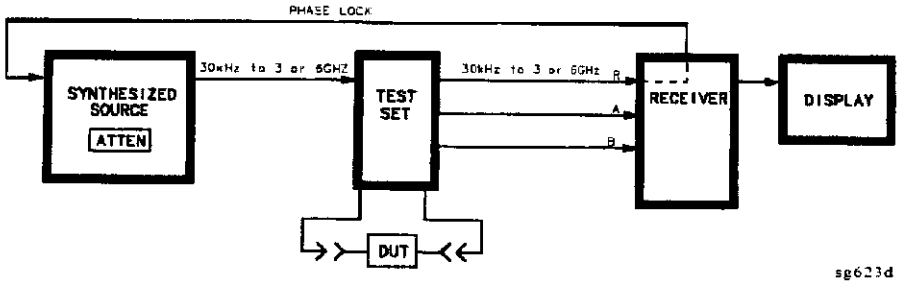


Figure 12-1. Simplified Block Diagram of the Network Analyzer System

The Built-In Synthesized Source

The analyzer's built-in synthesized source produces a swept RF signal in the range of 30 kHz to 3.0 GHz. The HP 8753E Option 006 is able to generate signals up to 6 GHz. The source output power is leveled by an internal ALC (automatic leveling control) circuit. To achieve frequency accuracy and phase measuring capability, the analyzer is phase locked to a highly stable crystal oscillator.

For this purpose, a portion of the transmitted signal is routed to the R channel input of the receiver, where it is sampled by the phase detection loop and fed back to the source.

The Source Step Attenuator

The 70 dB, electro-mechanical, step attenuator contained in the source has very low loss. It is used to adjust the power level to the device under test without changing the level of the incident power in the reference path. The user sets the attenuation levels via the front panel softkeys.

The Built-In Test Set

The HP 8753E features a built-in test set that provides the signal separation capability for the device under test, as well as to the signal-separation devices. The signal separation devices are needed to separate the incident signal from the transmitted and reflected signals. The incident signal is applied to the R channel input via an external jumper cable on the front panel. Meanwhile, the transmitted and reflected signals are internally routed from the test port couplers to the inputs of the A and B sampler/mixers in the receiver. Port 1 is connected to the A input and port 2 is connected to the B input.

The test set contains the hardware required to make simultaneous transmission and reflection measurements in both the forward and reverse directions. A solid-state transfer switch in the built-in test set allows reverse measurements to be made without changing the connections to the device under test.

The Receiver Block

The receiver block contains three sampler/mixers for the R, A and B inputs. The signals are sampled, and down-converted to produce a 4 kHz IF (intermediate frequency). A multiplexer sequentially directs each of the three IF signals to the ADC (analog to digital converter) where it is converted from an analog to a digital signal to be measured and processed for viewing on the display. Both amplitude and phase information are measured simultaneously, regardless of what is displayed on the analyzer.

The Microprocessor

A microprocessor takes the raw data and performs all the required error correction, trace math, formatting, sealing, averaging, and marker operations, according to the instructions from the front panel or over HP-IB The formatted data is then displayed.

Required Peripheral Equipment

In addition to the analyzer, a system requires calibration standards for vector accuracy enhancement, and cables for interconnections.

A Close Look at the Analyzer's Functional Groups

The operation of the analyzer is most logically described in five functional groups. Each group consists of several major assemblies, and performs a distinct function in the instrument. Some assemblies are related to more than one group, and in fact all the groups are to some extent interrelated and affect each other's performance.

Power Supply. The power supply functional group consists of the A8 post regulator and the A15 preregulator. It supplies power to the other assemblies in the instrument.

Digital Control. The digital control group consists of the A1 front panel and A2 front panel processor, the A9 CPU, the A16 rear panel, the A18 display and the A19 graphics system processor (GSP). The A10 digital IF assembly is also related to this group. These assemblies combine to provide digital control for the analyzer.

Source. The source group consists of the A3 source, A7 pulse generator, A11 phase lock, A12 reference, A13 fractional-N (analog), and A14 fractional-N (digital) assemblies. The A4 sampler is also related since it is part of the source phase lock loop. The source supplies a phase-locked RF signal to the device under test.

Signal Separation. The signal separation group performs the function of an S-parameter test set, dividing the source signal into a reference path and a test path, and providing connections to the device under test. It consists of the A24 transfer switch, the A21 test port 1 coupler, and the A22 test port 2 coupler.

Receiver. The receiver group consists of the A4/A5/A6 sampler/mixers and the A10 digital IF. The A12 reference assembly and the A9 CPU are also related. The receiver measures and processes input signals for display.

The following pages describe the operation of each of the functional groups.

Power Supply Theory

The power supply functional group consists of the A15 preregulator and the A8 post regulator. These two assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the analyzer. The A15 preregulator is enclosed in a casting at the rear of the instrument behind the display. It is connected to the A8 post regulator by a wire bus A15W1. Figure 12-2 is a simplified block diagram of the power supply group.

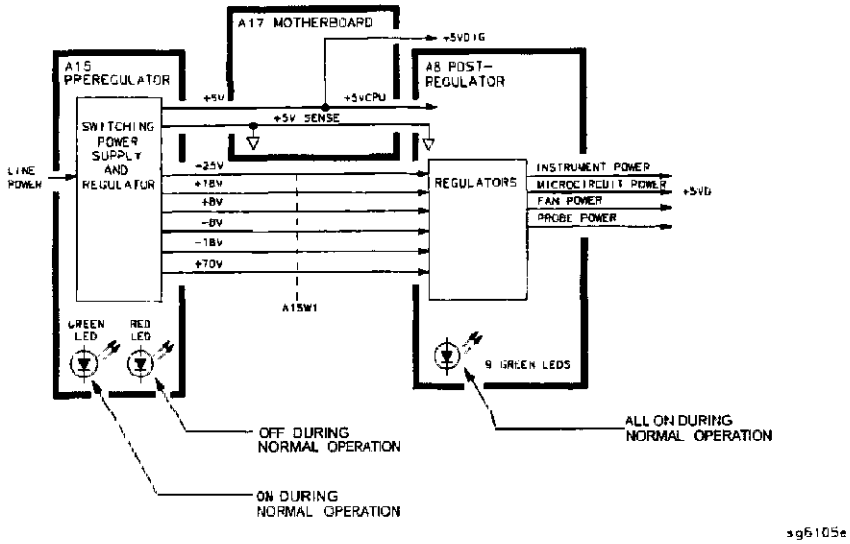


Figure 12-2. Power Supply Functional Group, Simplified Block Diagram

A15 Preregulator

The A15 preregulator steps down and rectifies the line voltage It provides a fully regulated +5 V digital supply, and several preregulated voltages that go to the A8 post regulator assembly for additional regulation.

The A15 preregulator assembly includes the line power module, a 60 kHz switching preregulator, and overvoltage protection for the +5 V digital supply. It provides LEDs, visible from the rear of the instrument, to indicate either normal or shutdown status.

Line Power Module

The line power module includes the line power switch, voltage selector switch, and main fuse. The line power switch is activated from the front panel. The voltage selector switch, accessible at the rear panel, adapts the analyzer to local line voltages of approximately 115 V or 230 V (with 350 VA maximum). The main fuse, which protects the input side of the preregulator against drawing too much line current, is also accessible at the rear panel. Refer to the *HP 8753E Network Analyzer Installation and Quick Start Guide* for line voltage tolerances and other power considerations.

Preregulated Voltages

The switching preregulator converts the line voltage to several DC voltages. The regulated +5 V digital supply goes directly to the motherboard. The following partially regulated voltages are routed through A15W1 to the A8 post regulator for final regulation:

+70V +25V +18V -18V +8V -8V

Regulated +5 V Digital Supply

The +5 VD supply is regulated by the control circuitry in the A15 preregulator. It goes directly to the motherboard, and from there to all assemblies requiring a low noise digital supply. A +5 V sense line returns from the motherboard to the A15 preregulator. The +5 V CPU is derived from the +5 VD in the A8 post regulator and goes directly to the A19 graphics system processor.

In order for the preregulator to function, the +5 V digital supply must be loaded by one or more assemblies, and the +5 V sense line must be working. If not, the other preregulated voltages will not be correct.

Shutdown Indications: the Green LED and Red LED

The green LED is on in normal operation. It is off when line power is not connected, not switched on, or set too low, or if the line fuse has blown.

The red LED, which is off in normal operation, lights to indicate a fault in the +5 V supply. This may be an over/under line voltage, over line current, or overtemperature condition. Refer to the troubleshooting chapters for more information.

A8 Post Regulator

The A8 post regulator filters and regulates the DC voltages received from the A15 preregulator. It provides fusing and shutdown circuitry for individual voltage supplies. It distributes regulated constant voltages to individual assemblies throughout the instrument. It includes the overtemperature shutdown circuit, the variable fan speed circuit, and the air flow detector. Nine green LEDs provide status indications for the individual voltage supplies.

Refer to the Power Supply Block Diagram located at the end of Chapter 5, "Power Supply Troubleshooting", to see the voltages provided by the A8 post regulator.

Voltage Indications: the Green LEDs

The nine green LEDs along the top edge of the A8 assembly are on in normal operation, to indicate the correct voltage is present in each supply. If they are off or flashing, a problem is indicated. The troubleshooting procedures later in this chapter detail the steps to trace the cause of the problem.

Shutdown Circuit

The shutdown circuit is triggered by overcurrent, overvoltage, undervoltage, or overtemperature. It protects the instrument by causing the regulated voltage supplies to be shut down. It also sends status messages to the A9 CPU to trigger warning messages on the analyzer display. The voltages that are not shut down are the +5 VD and +5 VCPU digital supplies from the preregulator, the fan supplies, the probe power supplies, and the display supplies. The shutdown circuit can be disabled momentarily for troubleshooting purposes by using a jumper to connect the SDIS line (A8TP4) to ground.

Variable Fan Circuit and Air Flow Detector

The fan power is derived directly from the + 18 V and -18 V supplies from the A15 preregulator. The fan is not fused, so that it will continue to provide airflow and cooling when the instrument is otherwise disabled. If overheating occurs, the main instrument supplies are shut down and the fan runs at full speed. An overtemperature status message is sent to the A9 CPU to initiate a warning message on the analyzer display. The fan also runs at full speed if the air flow detector senses a low output of air from the fan. (Full speed is normal at initial power on.)

Display Power

The A8 assembly supplies +5 VCPU to the A19 GSP through the motherboard. The GSP converts a portion of the +5 VCPU to 3.3 V to drive the display and LVDS (low voltage differential signaling) logic. The A19 GSP also controls and supplies power to the A27 backlight inverter The voltages generated by the inverter are then routed to the display. Display power is not connected to the protective shutdown circuitry so that the A18 display assemblies can operate during troubleshooting when other supplies do not work.

Note **If blanking pulses from the A19 GSP are not present, then +3.3 V will not be sent to the display.**

Probe Power

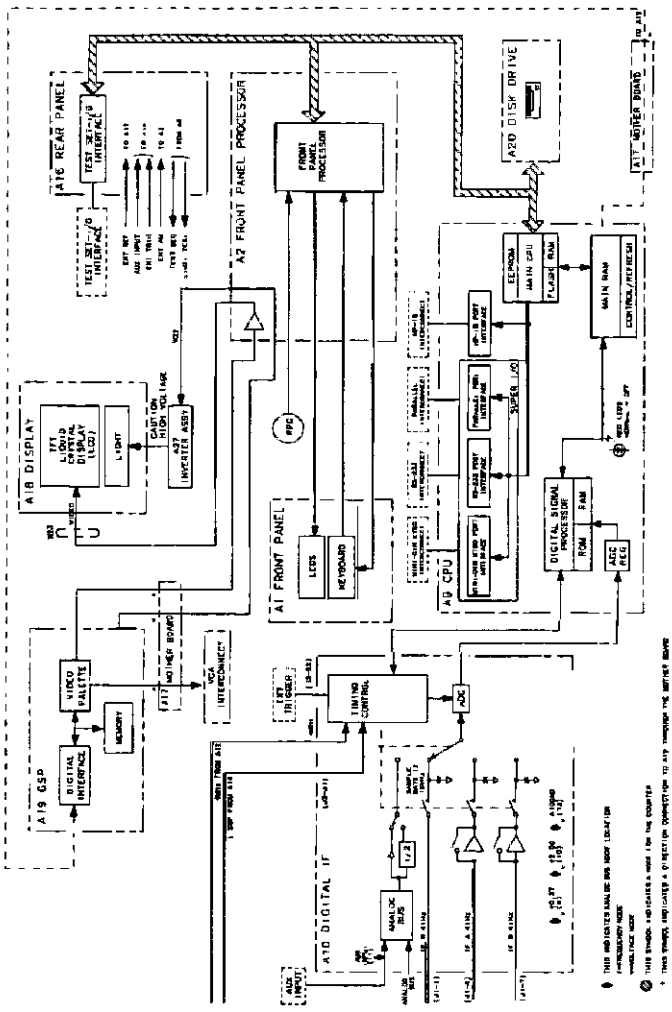
The +18 V and -18 V supplies are post regulated to +15 V and -12.6 V to provide a power source at the front panel for an external RF probe or millimeter modules.

Digital Control Theory

The digital control functional group consists of the following assemblies:

- A1 front panel
- A2 front panel processor
- A9 CPU
- A10 digital IF
- A16 rear panel
- A18 display
- A19 GSP
- A27 Inverter

These assemblies combine to provide digital control for the entire analyzer. They provide math processing functions, as well as communications between the analyzer and an external controller and/or peripherals Figure 12-3 is a simplified block diagram of the digital control functional group.



sg6107e

Figure 12-3. Digital Control Group, Simplified Block Diagram

A1 Front Panel

The A1 front panel assembly provides user interface with the analyzer. It includes the keyboard for local user inputs, and the front panel LEDs that indicate instrument status. The RPG (rotary pulse generator) is not electrically connected to the front panel, but provides user inputs directly to the front panel processor.

A2 Front Panel Processor

The A2 front panel processor detects and decodes user inputs from the front panel and the RPG, and transmits them to the CPU. It has the capability to interrupt the CPU to provide information updates. It controls the front panel LEDs that provide status information to the user.

The A2 also contains the LVDS (low voltage differential signaling) receivers which connect to the graphics processor. The received video signals are routed to the A18 display.

A9 CPU/A10 Digital IF

The A9 CPU assembly contains the main CPU (central processing unit), the digital signal processor, memory storage, and interconnect port interfaces. The main CPU is the master controller for the analyzer, including the other dedicated microprocessors. The memory includes EEPROM, DRAM, flash ROM, SRAM and boot ROM.

Data from the receiver is serially clocked into the A9 CPU assembly from the A10 digital IF. The data taking sequence is triggered either from the A14 fractional-N assembly, externally from the rear panel, or by software on the A9 assembly.

Main CPU

The main CPU is a 32-bit microprocessor that maintains digital control over the entire instrument through the instrument bus. The main CPU receives external control information from the front panel or HP-IB, and performs processing and formatting operations on the raw data in the main RAM It controls the digital signal processor, the front panel processor, the display processor, and the interconnect port interfaces. In addition, when the analyzer is in the system controller mode, the main CPU controls peripheral devices through the peripheral port interfaces.

The main CPU has a dedicated flash ROM that contains the operating system for instrument control. Front panel settings are stored in SRAM, with a battery providing at least 5 years of backup storage when external power is off.

Main RAM

The main RAM (random access memory) is shared memory for the CPU and the digital signal processor It stores the raw data received from the digital signal processor, while additional calculations are performed on it by the CPU. The CPU reads the resulting formatted data from the main RAM and converts it to GSP commands. It writes these commands to the GSP for output to the analyzer display

EEPROM

EEPROM (electrically-erasable programmable read only memory) contains factory set correction constants unique to each instrument. These constants correct for hardware variations to maintain the highest measurement accuracy. The correction constants can be updated by executing the routines in Chapter 3, "Adjustments and Correction Constants"

Digital Signal Processor

The digital signal processor receives the digitized data from the A10 digital IF. It computes discrete Fourier transforms to extract the complex phase and magnitude data from the 4 kHz IF signal. The resulting raw data is written into the main RAM.

A18 Display

The A18 display is an 8.4 inch LCD with associated drive circuitry. It receives a +3 3 V power supply from the A19 GSP, along with the voltage generated from the A27 backlight inverter. It receives the following signals from the A19 GSP:

- digital TTL horizontal sync
- digital TTL vertical sync
- blanking
- data clock
- digital TTL red video
- digital TTL green video
- digital TTL blue video

A19 GSP

The A19 graphics system processor is the main interface between the A9 CPU and the A18 display. The CPU (A9) converts the formatted data to GSP commands and writes it to the GSP. The GSP processes the data to obtain the necessary video signals, which are then used for the following purposes:

- The video signals are used to produce VGA compatible RGB output signals, which are routed to the A16 rear panel.
- The video signals are converted by an LVDS (low voltage differential signaling) driver which translates the signals to low level differential signals to help eliminate radiated emissions. The converted video signals are then routed to the A2 assembly, where they are received and sent to the A18 display.

The A19 assembly receives the +5 VCPU which is **used** for processing and supplying power to the A27 backlight inverter (+ 5 VCPU) and the A18 display (3.3 V).

A27 Inverter

The A27 backlight inverter assembly supplies the ac voltage for the backlight tube in the A18 display assembly. This assembly takes the + 5 VCPU and converts it to approximately 380 Vac with 5 ma of current at 40 kHz. There are two control lines:

- Digital ON/OFF
- Analog Brightness
  - 100% intensity is 0 V
  - 50% intensity is 4.5 V

A16 Rear Panel

The A16 rear panel includes the following interfaces:

TEST SET I/O INTERCONNECT. This provides control signals and power to operate duplexer test adapters.

EXT REF. This allows for a frequency reference signal input that can phase lock the analyzer to an external frequency standard for increased frequency accuracy.

The analyzer automatically enables the external frequency reference feature when a signal is connected to this input. When the signal is removed, the analyzer automatically switches back to its internal frequency reference.

10 MHZ PRECISION REFERENCE. (Option 1D5) This output is connected to the EXT REF (described above) to improve the frequency accuracy of the analyzer.

AUX INPUT. This allows for a dc or ac voltage input from an external signal source, such as a detector or function generator, which you can then measure, using the S-parameter menu. (You can also use this connector as an analog output in service routines.)

EXT AM. This allows for an external analog signal input that is applied to the ALC circuitry of the analyzer's source. This input analog signal amplitude modulates the RF output signal.

EXT TRIG. This allows connection of an external negative TTL-compatible signal that will trigger a measurement sweep. The trigger can be set to external through softkey functions.

TEST SEQ. This outputs a TTL signal that can be programmed in a test sequence to be high or low, or pulse (10 μseconds) high or low at the end of a sweep for a robotic part handler interface.

LIMIT TEST. This outputs a TTL signal of the limit test results as follows:

Pass: TTL high

Fail: TTL low

VGA OUTPUT. This provides a video output of the analyzer display that is capable of running a PC VGA monitor.

Source Theory Overview

The source produces a highly stable and accurate RF output signal by phase locking a YIG oscillator to a harmonic of the synthesized VCO (voltage controlled oscillator). The source output produces a CW or swept signal between 300 kHz and 3 GHz (or 300 kHz and 6 GHz for Option 006) with a maximum leveled power of + 10 dBm. The source's built-in 70 dB step attenuator allows the power to go as low as -85 dBm.

The full frequency range of the source is produced in 14 subsweeps, one in super low band, two in low band, and eleven in high band. The high band frequencies (16 MHz to 3 GHz) or (16 MHz to 6 GHz for Option 006) are achieved by harmonic mixing, with a different harmonic number for each subsweep. The low band frequencies (300 kHz to 16 MHz) are down-converted by fundamental mixing. The super low band frequencies (10 kHz to 300 kHz) are sent directly from the A12 reference board to the output of the A3 source assembly. This band is not phased locked nor does it use the ALC. It is the basic amplified output of the fractional-N synthesizer.

The source functional group consists of the individual assemblies described below.

A14/A13 Fractional-N

These two assemblies comprise the synthesizer. The 30 to 60 MHz VCO in the A14 assembly generates the stable LO frequencies for fundamental and harmonic mixing.

A12 Reference

This assembly provides stable reference frequencies to the rest of the instrument by dividing down the output of a 40 MHz crystal oscillator. In low band operation, the output of the fractional-N synthesizer is mixed down in the A12 reference assembly. (The 2nd LO signal from the A12 assembly is explained in Receiver Theory.) The A12 is also the origin of the super low band portion of the 8753E source.

A7 Pulse Generator

A step recovery diode in the pulse generator produces a comb of harmonic multiples of the VCO output. These harmonics provide the high band LO (local oscillator) input to the samplers. In low band and super low band the operation the pulse generator is turned off.

A11 Phase Lock

This assembly compares the first IF (derived from the source output in the A4 sampler) to a stable reference, and generates an error voltage that is integrated into the drive for the A3 source assembly.

A3 Source

This assembly includes a 3.0 to 6.8 GHz YIG oscillator and a 3.8 GHz cavity. oscillator The outputs of these oscillators are mixed to produce the RF output signal. In Option 006 (30 kHz to 6 GHz) the frequencies 3.0 to 6.0 GHz are no longer a mixed product, but are the direct output of the YIG Oscillator. The signal tracks the stable output of the synthesizer. The ALC (automatic leveling control) circuitry is also in the A3 assembly.

Source Super Low Band Operation

The Super Low Band Frequency Range is 10 kHz to 300 kHz. These frequencies are generated by the A12 Reference Board. They are the amplified output of the fractional-N synthesizer. This output is not phase locked and is not subject to ALC control. Refer to Table 12-1.

Table 12-1. Super Low Band Subsweep Frequencies

Fractional-N (MHz)	1st IF (MHz)	RF Output (MHz)
40.0 to 43.3	0.010 to 0.300	0.010 to 0.300

Source Low Band Operation

The low band frequency range is 300 kHz to 16 MHz. These frequencies are generated by locking the A3 source to a reference signal. The reference signal is synthesized by mixing down the fundamental output of the fractional-N VCO with a 40 MHz crystal reference signal. Low band operation differs from high band in these respects: The reference frequency for the All phase lock is not a fixed 1 MHz signal, but varies with the frequency of the fractional-N VCO signal. The sampler diodes are biased on to pass the signal through to the mixer. The 1st IF signal from the A4 sampler is not fixed but is identical to the source output signal and sweeps with it. The following steps outline the low band sweep sequence, illustrated in Figure 12-4.

1. **A signal (FN LO) is generated by the fractional-N VCO.** The VCO in the Al4 Fractional-N assembly generates a CW or swept signal that is 40 MHz greater than the start frequency. The signal is divided down to 100 kHz and phase locked in the Al3 assembly, as in high band operation.
2. **The fractional-N VCO signal is mixed with 40 MHz to produce a reference signal.** The signal (FN LO) from the Fractional-N VCO goes to the Al2 reference assembly, where it is mixed with the 40 MHz VCXO (voltage controlled crystal oscillator). The resulting signal is the reference to the phase comparator in the All assembly.
3. **The A3 source is pretuned. The source output is fed to the A4 sampler.** The pretuned DAC in the All phase lock assembly sets the A3 source to a frequency 1 to 6 MHz above the start frequency. This signal (source output) goes to the A4 R input sampler/mixer assembly.
4. **The signal from the source is fed back (1st IF) to the phase comparator.** The source output signal passes directly through the sampler in the A4 assembly, because the sampler is biased on. The signal (1st IF) is fed back unaltered to the phase comparator in the All phase lock assembly. The other input to the phase comparator is the heterodyned reference signal from the Al2 assembly. Any frequency difference between these two signals produces a proportional error voltage.
5. **A tuning signal (YO DRIVE) tunes the source and phase lock is achieved.** The error voltage is used to drive the A3 source YIG oscillator to bring the YIG closer to the reference frequency. The loop process continues until the source frequency and the reference frequency are the same, and phase lock is achieved.

6. **A synthesized sub sweep is generated. The source tracks the synthesizer.** When lock is achieved at the start frequency, the synthesizer starts to sweep. This changes the phase lock reference frequency, and causes the source to track at a difference frequency 40 MHz below the synthesizer.

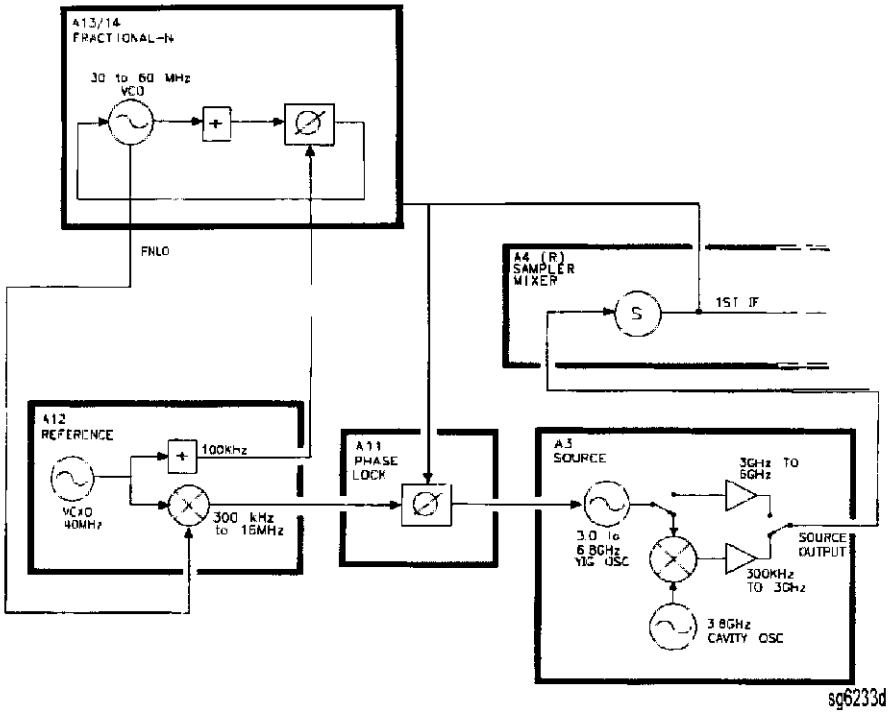


Figure 12-4. Low Band Operation of the Source

The full low band is produced in two sub sweeps, to allow addition IF filtering below 3 MHz. At the transition between subsweeps, the source is pretuned and then relocks. Table 12-2 lists the low band subsweep frequencies at the fractional-N VCO and the RF output.

TAble 12-2. Low Band Subsweep Frequencies

Fractional-N (MHz)	1st IF (MHz)	Source Output (MHz)
40.3 to 43.3	0.3 to 3.3	0.3 to 3.3
43.3 to 56.0	3.3 to 16.0	3.3 to 16.0

Source High Band Operation

The high band frequency range is 16 MHz to 3.0 GHz or 16 MHz to 6.0 GHz with Option 006. These frequencies are generated in subsweeps by phase-locking the A3 source signal to harmonic multiples of the fractional-N VCO. The high band subsweep sequence, illustrated in Figure 12-5, follows these steps:

1. **A signal (III OUT) is generated by the fractional-N VCO.** The VCO in the A14 fractional-N assembly generates a CW or swept signal in the range of 30 to 60 MHz. This signal is synthesized and phase locked to a 100 kHz reference signal from the A12 reference assembly. The signal from the fractional-N VCO is divided by 1 or 2, and goes to the pulse generator.
2. **A comb of harmonics (1st LO) is produced in the A7 pulse generator.** The divided down signal from the fractional-N VCO drives a step recovery diode (SRD) in the A7 pulse generator assembly. The SRD multiplies the fundamental signal from the fractional-N into a comb of harmonic frequencies. The harmonics are used as the 1st LO (local oscillator) signal to the samplers. One of the harmonic signals is 1 MHz below the start signal set from the front panel.
3. **The A3 source is pretuned. The source output is fed to the A4 sampler.** The pretune DAC in the A11 phase lock assembly sets the A3 source to a first approximation frequency (1 to 6 MHz higher than the start frequency). This signal (RF OUT) goes to the A4 R input sampler/mixer assembly.
4. **The synthesizer signal and the source signal are combined by the sampler. A difference frequency is generated.** In the A4 sampler, the 1st LO signal from the pulse generator is combined with the source output signal. The IF (intermediate frequency) produced is a first approximation of 1 MHz. This signal (1st IF) is routed back to the A11 phase lock assembly.
5. **The difference frequency (1st IF) from the A4 sampler is compared to a reference.** The 1st IF feedback signal from the A4 is filtered and applied to a phase comparator circuit in the A11 phase lock assembly. The other input to the phase comparator is a crystal controlled 1 MHz signal from the A12 reference assembly. Any frequency difference between these two signals produces a proportional error voltage
6. **A tuning signal (YO DRIVE) tunes the source and phase lock is achieved.** The error voltage is used to drive the A3 source YIG oscillator, in order to bring it closer to the required frequency. The loop process continues until the 1st IF feedback signal to the phase comparator is equal to the 1 MHz reference signal, and phase lock is achieved.

7. **A synthesized subsweep is generated by A13/A14. The A3 source tracks the synthesizer.** When the source is phase locked to the synthesizer at the start frequency, the synthesizer starts to sweep. The phase locked loop forces the source to track the synthesizer, maintaining a constant 1 MHz 1st IF signal.

   The full high band sweep is generated in a series of subsweeps, by phase locking the A3 source signal to harmonic multiples of the fractional-N VCO. The 16 to 31 MHz subsweep is produced by a one half harmonic, using the divide-by-2 circuit on the A14 assembly. At the transitions between subsweeps, the source is pretuned and then relocks. Table 12-3 lists the high band subsweep frequencies from the fractional-N VCO and the source output.

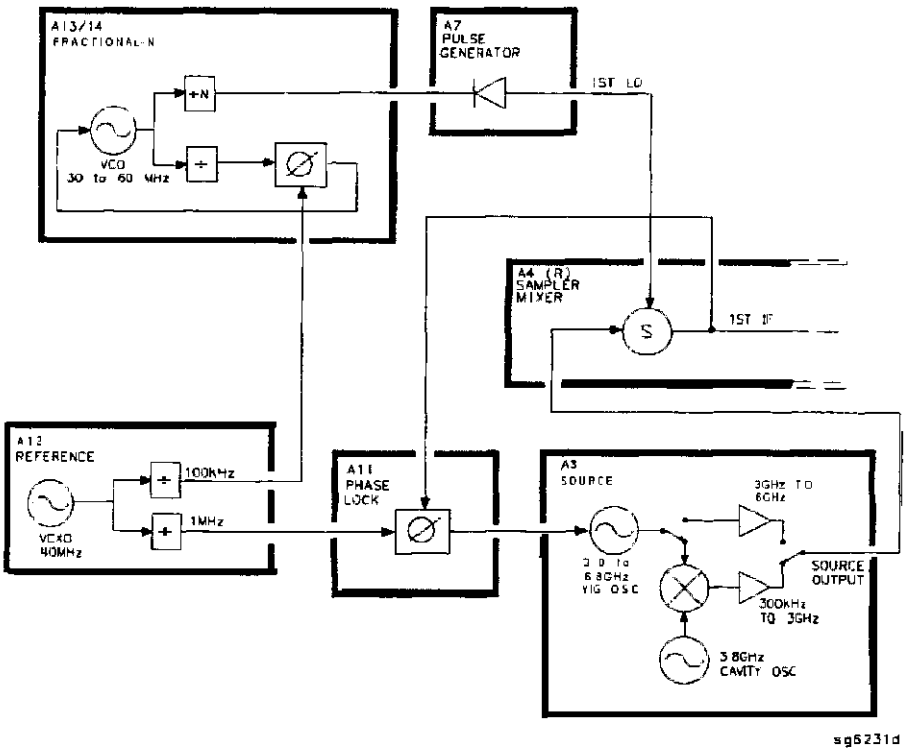


Figure 12-5. High Band Operation of the Source

Table 12-3. High Band Subsweep Frequencies

Fractional-N (MHz)	Harmonic	Source Output (MHz)
30 to 60	1/2	16 to 31
30 to 60	1	31 to 61
30 to 60	2	61 to 121
40 to 59	3	121 to 178
35.4 to 59.2	5	178 to 296
32.8 to 59.4	9	296 to 536
35.7 to 59.5	15	536 to 893
33.0 to 59.5	27	893 to 1607
31.5 to 58.8	51	1607 to 3000
Option 006		
37.0 to 59.6	83	3000 to 4950
49.0 to 59.4	101	4950 to 6000

Source Operation in other Modes/Features

Besides the normal network analyzer mode, the HP 8753E has extra modes and features to make additional types of measurements. The following describes the key differences in how the analyzer operates to achieve these new measurements.

Frequency Offset

The analyzer can measure frequency-translating devices with the frequency offset feature.

The receiver operates normally. However, the source is pretuned to a different frequency by an offset entered by the user. The device under test will translate this frequency back to the frequency the receiver expects. Otherwise, phase locking and source operation occur as usual.

Harmonic Analysis (Option 002)

The analyzer can measure the 2nd or 3rd harmonic of the fundamental source frequency, on a swept or CW basis, with the harmonic analysis feature (optional).

To make this measurement, the reference frequency (normally 1 MHz) from the A12 reference assembly to the A11 phase lock assembly is divided by 1, 2, or 3. See Figure 12-6.

The fractional-N assemblies are also tuned so that the correct harmonic (comb tooth) of the 1st LO is 0.500 or 0.333 MHz below the source frequency instead of the usual 1 000 MHz. The analyzer pretunes the A3 source normally, then phase locks the 1st IF to the new reference frequency to sweep the fundamental source frequency in the usual way. The key difference is that the 1st IF (output from the R sampler) due to the fundamental and used for phase locking is now 0.500 or 0.333 MHz instead of 1.000 MHz.

Since the chosen VCO harmonic and the source differ by 0.500 or 0.333 MHz, then another VCO harmonic, 2 or 3 times higher in frequency, will be exactly 1.000 MHz away from the 2nd or 3rd harmonic of the source frequency. The samplers, then, will also down-convert these harmonics to yield the desired components in the 1st IF at 1.000 MHz. Narrow bandpass filters in the receiver eliminate all but the 1.000 MHz signals; these pass through to be processed and displayed.

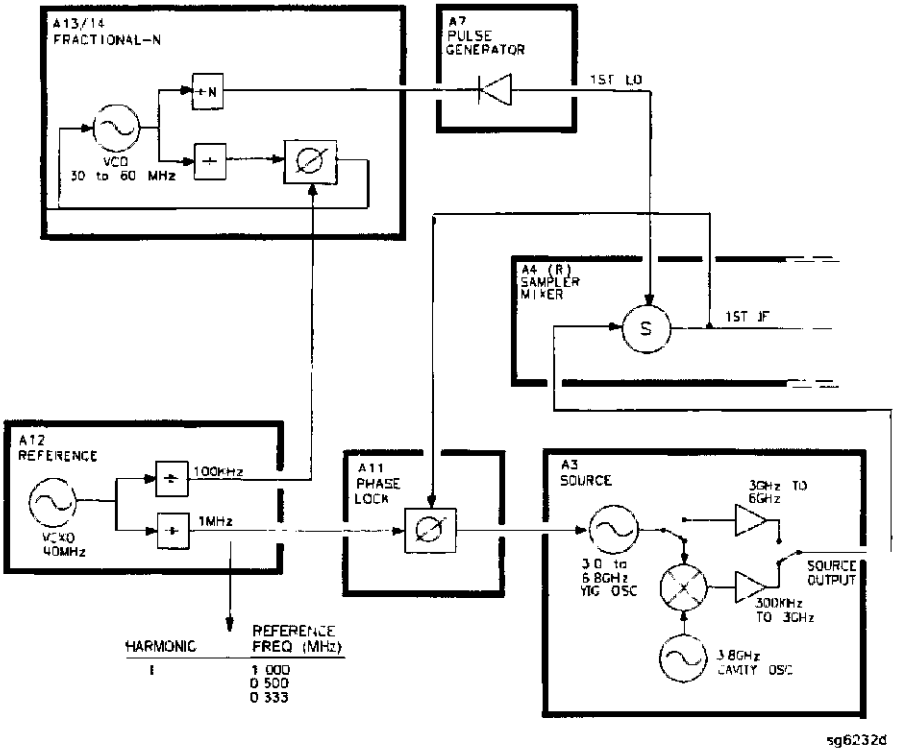


Figure 12-6. Harmonic Analysis

External Source Mode

In external source mode, the analyzer phase locks its receiver to an external signal source. This source must be CW (not swept), but it does not need to be synthesized. The user must enter the source frequency into the analyzer. (The analyzer's internal source output is not used.)

To accomplish this, the phase lock loop is reconnected so that the tuning voltage from the All phase lock assembly controls the VCO of the Al4 fractional-N assembly and not the A3 source See Figure 12-7 The VCO's output still drives the 1st LO of the samplers and down-converts the RF signal supplied by the external source. The resulting 1st IF is fed back to the All phase lock assembly,

compared to the 1.000 MHz reference, and used to generate a tuning voltage as usual. However, the tuning voltage controls the VCO to lock on to the external source, keeping the 1st IF at exactly 1.000 MHz.

The analyzer normally goes through a pretune-acquire-track sequence to achieve phase lock. In external source mode, the fractional-N VCO pretunes as a closed-loop synthesizer referenced to the 100 kHz signal from the A12 reference assembly. Then, to acquire or track, a switch causes the VCO to be tuned by the A11 phase lock assembly instead. (Refer to the Overall Block Diagram at the end of Chapter 4, "Start Troubleshooting Here.")

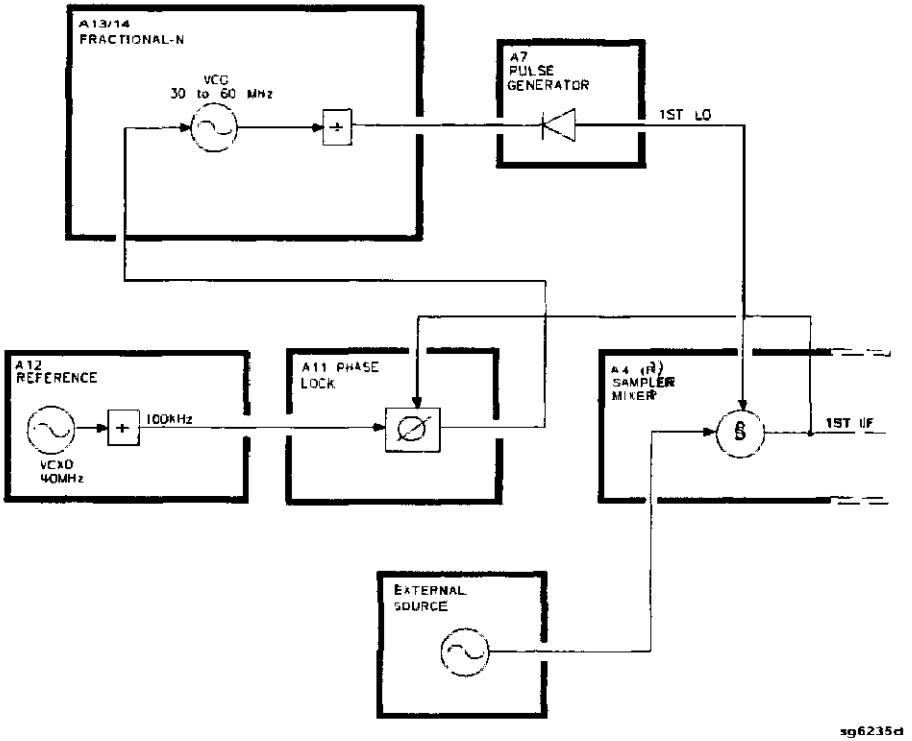


Figure 12-7. External Source Mode

Tuned Receiver Mode

In tuned receiver mode, the analyzer is a synthesized, swept, narrow-band receiver only. The external signal source must be synthesized and reference-locked to the analyzer.

To achieve this, the analyzer's source and phase lock circuits are completely unused. See Figure 12-8. The fractional-N synthesizer is tuned so that one of its harmonics (1st LO) down-converts the RF input to the samplers. (In contrast to external source mode, the analyzer does not phase lock at all. However, the 1st LO is synthesized.)

The analyzer can function as a swept tuned receiver, similar to a spectrum analyzer, but the samplers create spurious signals at certain frequencies, which limit the accuracy of such measurements.

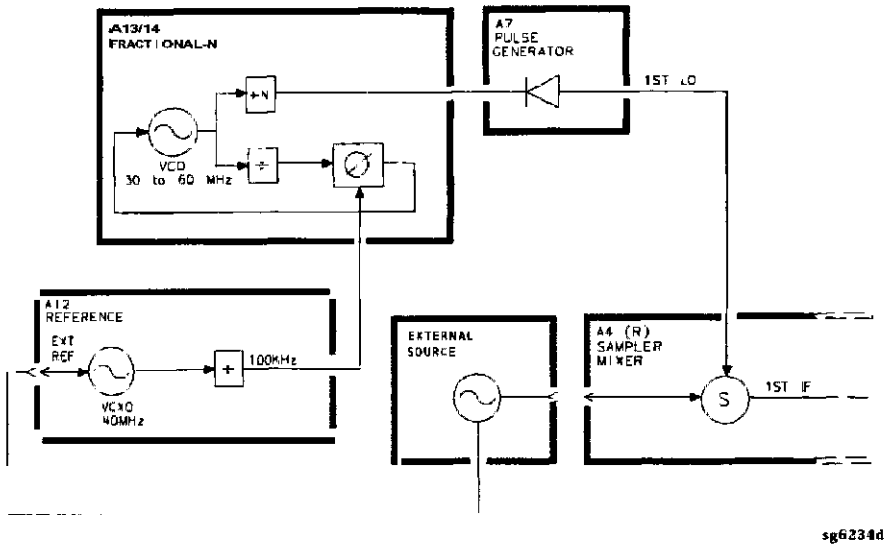


Figure 12-8. Tuned Receiver Mode

Signal Separation

The Built-In Test Set

Figure 12-9 shows a simplified block diagram of the analyzer's built-in test set.

A21 and A22 Test Port Couplers

The analyzer's test port couplers are used to separate signals incident to, reflected from, and transmitted from the device under test. Each test port coupler has a coupling coefficient factor of 16 dB.

A23 LED Front Panel

The LED front panel board indicates whether the source power is incident on the analyzer's test port 1 or test port 2. The analyzer's source power is directed to test port 1 when making a forward transmission/reflection measurement. Similarly, source power is incident at test port 2 when making a reverse transmission/reflection measurement.

A24 Transfer Switch

The A3 source output power is directed to either the analyzer's test port 1 or test port 2 via a low loss solid state transfer switch. With this switch, all four S-parameters can be updated continuously (for example: the data obtained from a full 2-port calibration). In addition, the transfer switch provides termination for the inactive test port in order to minimize the crosstalk between the source and receiver sampler.

A25 Test Set Interface

The test set interface board provides biasing for active devices under test, with an external dc voltage. This dc voltage is applied directly to the test port center pin. In addition, the test set interface board provides the drive signal for the A24 forward/reverse transfer switch.

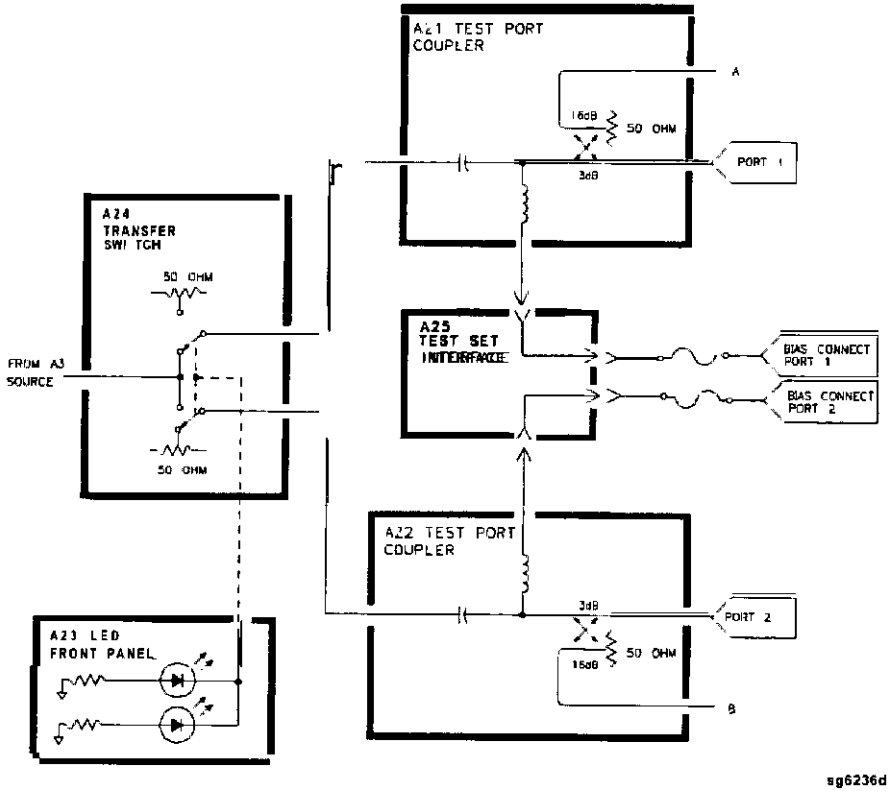


Figure 12-9. Simplified Block Diagram of the Built-in Test Set

Receiver Theory

The receiver functional group consists of the following assemblies:

A4 sampler/mixer

A5 sampler/mixer

A6 sampler/mixer

A10 digital IF

These assemblies combine with the A9 CPU (described in Digital Control Theory) to measure and process input signals into digital information for display on the analyzer. Figure 12-10 is a simplified block diagram of the receiver functional group. The A12 reference assembly is also included in the illustration to show how the 2nd LO signal is derived.

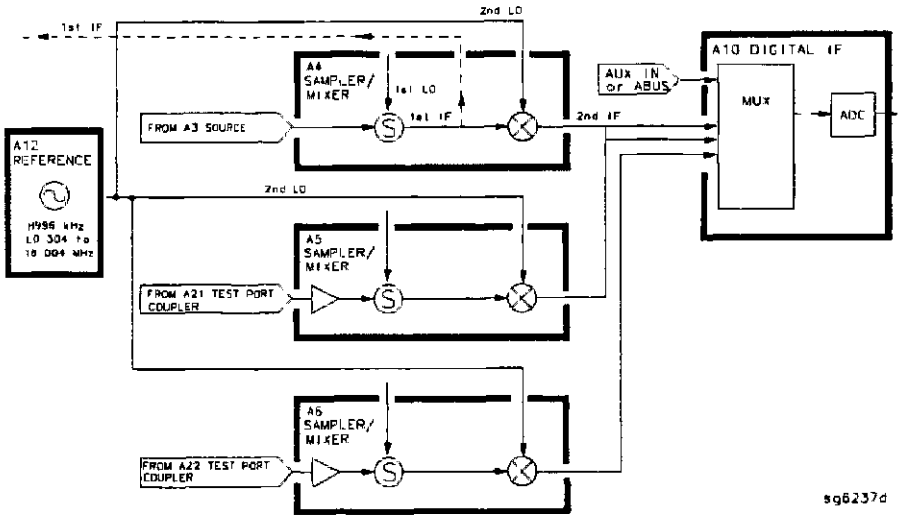


Figure 12-10. Receiver Functional Group, Simplified Block Diagram

A4/A5/A6 Sampler/Mixer

The A4, A5, and A6 sampler/mixers all down-convert the RF input signals to fixed 4 kHz 2nd IF signals with amplitude and phase corresponding to the RF input. The A5 and A6 sampler/mixer assemblies both include an 8 dB gain preamplifier in front of the sampler. This improves the noise figure performance of the analyzer's receiver channels A and B.

The Sampler Circuit in High Band

In high band operation, the sampling rate of the samplers is controlled by the 1st LO from the A7 pulse generator assembly. The 1st LO is a comb of harmonics produced by a step recovery diode driven by the fractional-N VCO fundamental signal. One of the harmonic signals is 1 MHz below the start frequency set at the front panel. The 1st LO is combined in the samplers with the RF input signal from the source. In the Option 006, samplers are additionally capable of recognizing RF input signals from 3 to 6 GHz. The mixing products are filtered, so that the only remaining response is the difference between the source frequency and the harmonic 1 MHz below it. This fixed 1 MHz signal is the 1st IF. Part of the 1st IF signal from the R sampler is fed back to the A11 phase lock assembly.

The Sampler Circuit in Low Band or Super Low Band

In low band or super low band the sampler diodes are biased continuously on, so that the RF input signal passes through them unchanged. Thus the 1st IF is identical to the RF output signal from the source (300 kHz to 16 MHz for lowband; 10 to 300 kHz for super lowband), and sweeps with it. Part of the 1st IF signal from the R sampler is fed back to the A11 phase lock assembly.

(Refer to "Source Theory Overview" for information on high band and low band operation of the source.)

The 2nd LO Signal

The 2nd LO is obtained from the A12 reference assembly. In high band, the 2nd LO is fixed at 996 kHz. This is produced by feeding the 39.84 MHz output of a phase-locked oscillator in the A12 assembly through a divide-by-40 circuit.

In low band, the 2nd LO is a variable frequency produced by mixing the output of the fractional-N VCO with a fixed 39.996 MHz signal in the A12 assembly. The 2nd LO covers the range of 0.014 to 16.004 MHz in two subsweeps that correspond with the source subsweeps. These subsweeps are 0.304 to 3.304 MHz and 3.304 to 16.004 MHz.

The Mixer Circuit

The 1st IF and the 2nd LO are combined in tne mixer circuit. The resulting difference frequency (the 2nd IF) is a constant 4 kHz in both bands, as Table 12-4 shows.

Table 12-4. Mixer Frequencies

Band	1st IF	2nd LO	2nd IF
Super Low	0.010 to 0.300 MHz	0.014 to 0.304 MHz	4.0 kHz
Low	0.300 to 16.0 MHz	0.304 to 16.004 MHz	4 0 kHz
High	1.000 MHz	0.996 MHz	4 0 kHz

Al0 Digital IF

The three 4 kHz 2nd IF signals from the sampler/mixer assemblies are input to the Al0 digital IF assembly. These signals are sampled at a 16 kHz rate. A fourth input is the analog bus, which can monitor either an external input at the rear panel AUX IN connector, or one of 31 internal nodes. A multiplexer sequentially directs each of the signals to the ADC (analog-to-digital converter). Here they are converted to digital form and sent to the A9 CPU assembly for processing. Refer to "Digital Control Theory" for more information on signal processing.

13

Replaceable Parts

This chapter contains information for ordering replacement parts for the HP 8753E network analyzer. Replaceable parts include the following:

- major assemblies
- cables
- chassis hardware

In general, parts of major assemblies are not listed. Refer to Table 13-1 at the back of this chapter to help interpret part descriptions in the replaceable parts lists that follow.

Replacing an Assembly

The following steps show the sequence to replace an assembly in an HP 8753E network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Rebuilt-Exchange Assemblies

Under the rebuilt-exchange assembly program, certain factory-repaired and tested modules (assemblies) are available on a trade-in basis. These assemblies are offered for lower cost than a new assembly, but meet all factory specifications required of a new assembly.

The defective assembly must be returned for credit under the terms of the rebuilt-exchange assembly program. Any spare assembly stock desired should be ordered using the new assembly part number. Figure 13-1 illustrates the module exchange procedure. "Major Assemblies, Top" and "Major Assemblies, Bottom" list all major assemblies, including those that can be replaced on an exchange basis.

Ordering Information

To order a part listed in the replaceable parts lists, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

To order a part that is not listed in the replaceable parts lists, include the instrument model number, complete instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

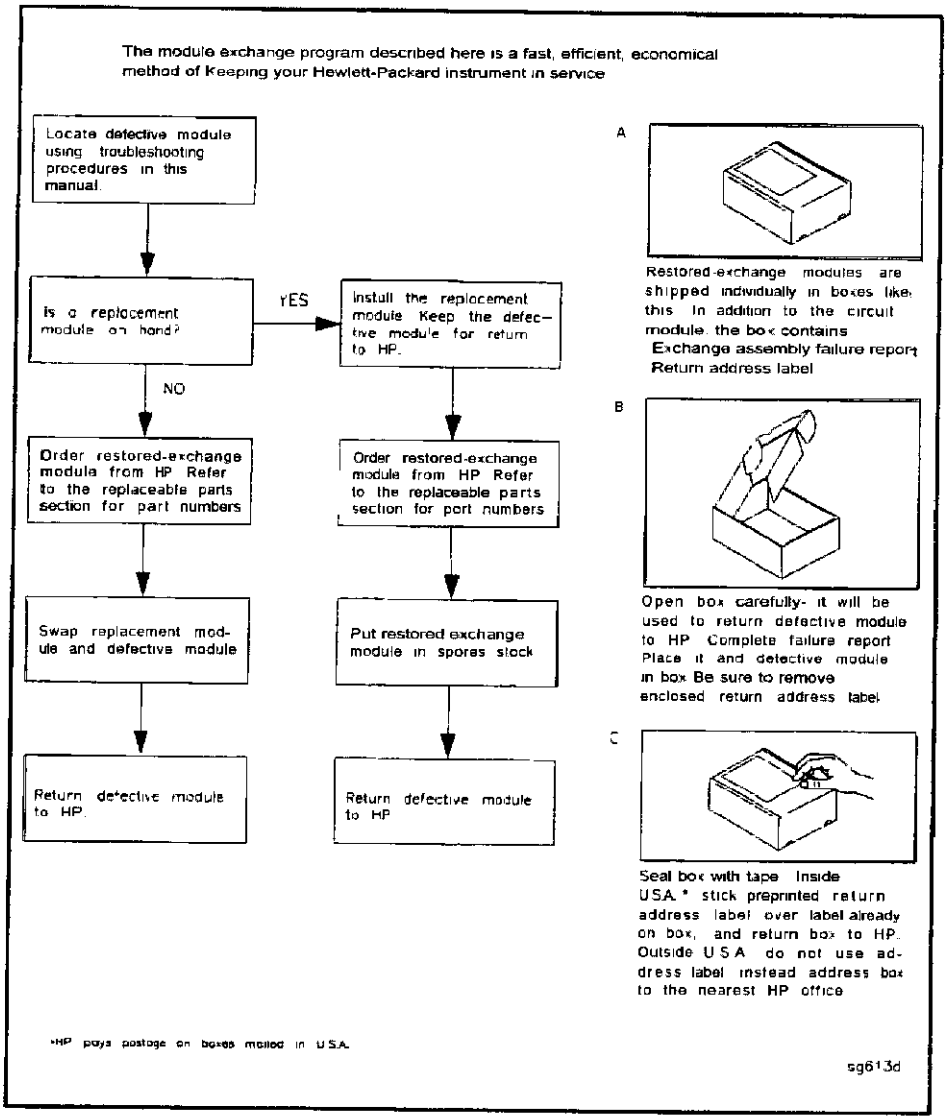


Figure 13-1. Module Exchange Procedure

Replaceable Part Listings

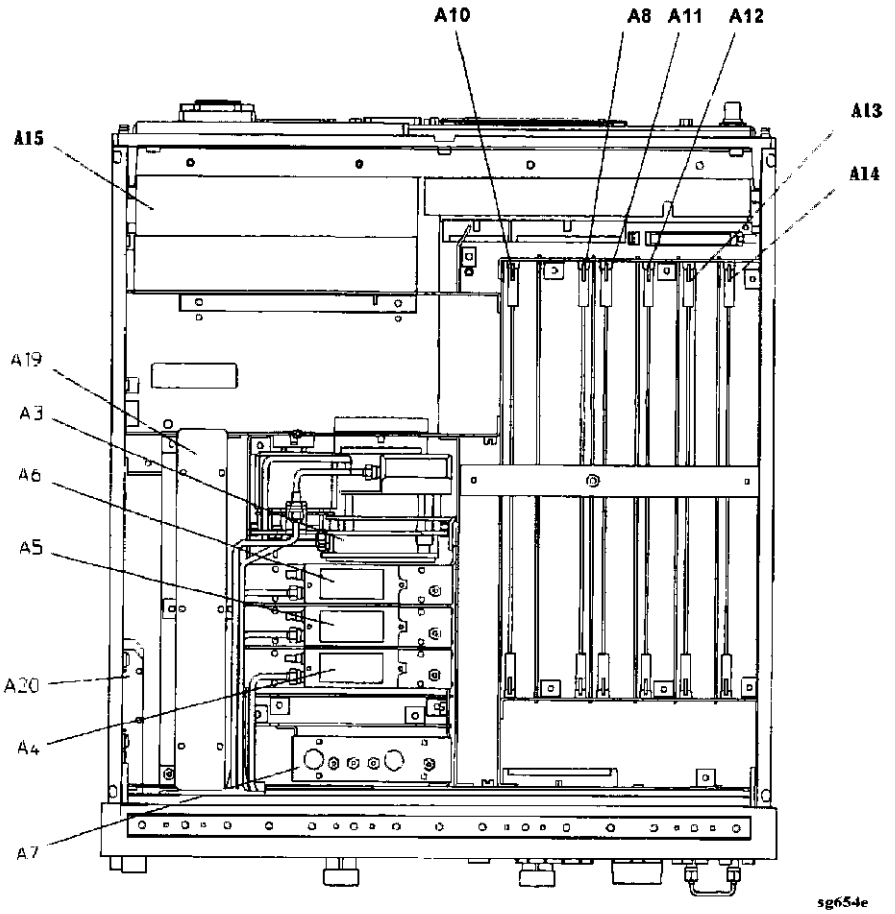
The following pages list the replacement part numbers and descriptions for the HP 8753E Network Analyzer. Illustrations with reference designators are provided to help identify and locate the part needed. The parts lists are organized into the following categories:

- Major Assemblies, Top
- Major Assemblies, Bottom
- Cables, Top
- Cables, Bottom
- Cables, Front
- Cables, Rear
- Cables, Source
- Front Panel, Outside
- Front Panel, Inside
- Rear Panel
- Rear Panel, Option 1D5
- Hardware, Top
- Hardware, Bottom
- Hardware, Front
- Hardware, Test Set Deck
- Hardware, Disk Drive Support
- Hardware, Memory Deck
- Hardware, Preregulator
- Chassis Parts, Outside
- Chassis Parts, Inside
- Miscellaneous

Major Assemblies, Top

Ref. Desig.	Option	HP Part Number	Qty	Description
A1				NOT SHOWN (see "Front Panel Assembly, Inside")
A2				NOT SHOWN (see "Front Panel Assembly, Inside")
A3		08763-60231	1	ASSY-SOURCE 3 GHz
A3		08753-69231	1	ASSY-SOURCE 3 GHz (REBUILT-EXCHANGE)
A3	006	08753-60146	1	ASSY-SOURCE 6 GHz
A3	006	08753-69146	1	ASSY-SOURCE 6 GHz (REBUILT-EXCHANGE)
A4		08753-60004	1	ASSY-SAMPLER R
A4		08753-69004	1	ASSY-SAMPLER R (REBUILT-EXCHANGE)
A5		08753-60169	1	ASSY-SAMPLER A
A5		08753-69169	1	ASSY-SAMPLER A (REBUILT-EXCHANGE)
A6		08753-60169	1	ASSY-SAMPLER B
A6		08753-69169	1	ASSY-SAMPLER B (REBUILT-EXCHANGE)
A7		08753-60164	1	BD ASSY-PULSE GENERATOR
A7		08753-69164	1	BD ASSY-PULSE GENERATOR (REBUILT-EXCHANGE)
A8*		08753-60208	1	BD ASSY-POST REGULATOR
A10		08753-60095	1	BD ASSY-DIGITAL IF
A11		08753-60162	1	BD ASSY-PHASE LOCK
A12		08753-60209	1	BD ASSY-REFERENCE
A13		08753-60013	1	BD ASSY-FRAC N ANALOG
A14		08753-60068	1	BD ASSY-FRAC N DIGITAL
A15		08753-60098	1	ASSY-PREREGULATOR
A15		08753-69098	1	ASSY-PREREGULATOR (REBUILT-EXCHANGE)
A16				NOT SHOWN (see "Rear Panel Assembly")
A17				NOT SHOWN (see "Chassis Parts, Inside")
A18			1	NOT SHOWN (see "Front Panel Assembly, Inside")
A19		08753-60271	1	BD ASSY-GRAPHICS PROCESSOR (under sheet metal cover)
A20		0950-3109	1	ASSY-DISK DRIVE
A27			1	NOT SHOWN (see "Front Panel Assembly, Inside")
A26	1D5			NOT SHOWN (see "Rear Panel Assembly, Option 1D5")
B1				NOT SHOWN (see "Rear Panel Assembly")
RPG				NOT SHOWN (see "Front Panel Assembly, Inside")

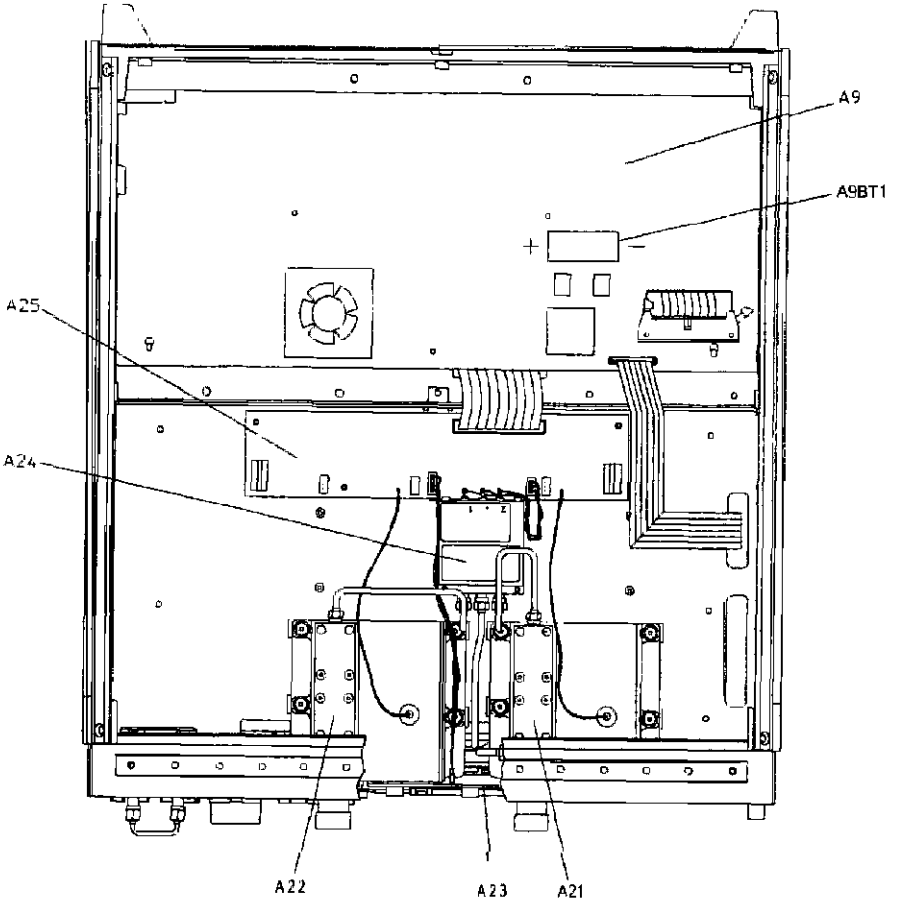
* For fuse part numbers on the A8 Post Regulator, refer to "Miscellaneous" in this chapter.


A10
A8
A11
A12
A13
A14
A15
A19
A3
A6
A5
A20
A4
A7
sg654e

Major Assemblies, Bottom

Ref. Desig.	Option	HP Part Number	Qty	Description
A9		08753-60272	1	BD ASSY-CPU/PIG
A9BT1		1420-0338	1	BATTERY-LITHIUM 3V 1.2AH
A21		6087-7007	1	ASSY-TEST PORT COUPLER
A21		5087-6007	1	ASSY-TEST PORT COUPLER (REBUILT-EXCHANGE)
A21	075	5087-7008	1	ASSY-TEST PORT COUPLER
A21	075	5087-6008	1	ASSY-TEST PORT COUPLER (REBUILT-EXCHANGE)
A22		5087-7007	1	ASSY-TEST PORT COUPLER
A22		5087-6007	1	ASSY-TEST PORT COUPLER (REBUILT-EXCHANGE)
A22	076	5087-7008	1	ASSY-TEST PORT COUPLER
A22	075	5087-6008	1	ASSY-TEST PORT COUPLER(REBUILT-EXCHANGE)
A23		08753-60145	1	BD ASSY-LED FRONT PANEL
A24		5086-7539	1	ASSY-TRANSFER SWITCH
A24		5086-6539	1	ASSY-TRANSFER SWITCH (REBUILT-EXCHANGE)
A25		08753-60280	1	BD ASSY-TEST SET INTERFACE

Major Assemblies, Bottom

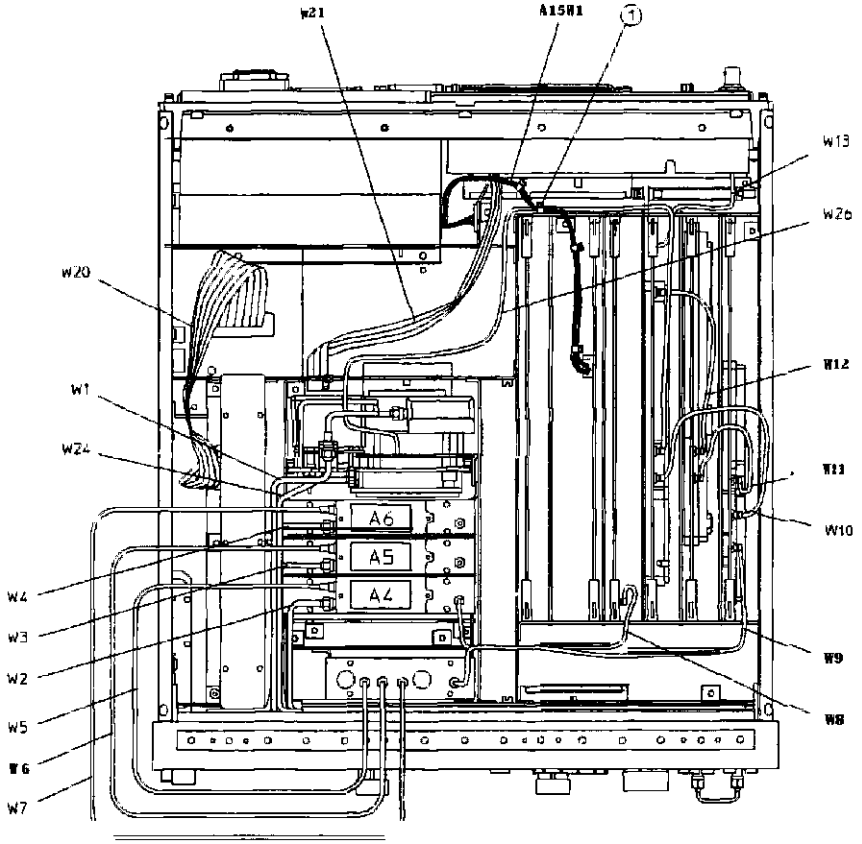


sg655e

Cables, Top

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
1			1400-0249	1	CABLE TIE (15W1 to CHASSIS)
A15W1	18W		(part of A15)	1	PREREGULATOR (A15) to POST REGULATOR (A8J2) and MOTHERBOARD (A17J8)
W1	SR		08753-20285	1	SOURCE ASSY (A3W4) to TRANSFER SWITCH (A24)
W2	SR		08753-20291	1	FP (R CHANNEL IN) to SAMPLER-R (A4)
W3	SR		08753-20286	1	TEST PORT 1 COUPLER (A21) to SAMPLER-A (A5)
W4	SR		08753-20287	1	TEST PORT 2 COUPLER (A22) to SAMPLER-B (A6)
W5	F		08753-60027	1	SAMPLER-R (A4) to PULSE GENERATOR (A7)
W6	F		08753-60027	1	SAMPLER-A (A5) to PULSE GENERATOR (A7)
W7	F		08753-60027	1	SAMPLER-B (A6) to PULSE GENERATOR (A7)
W8	F		08753-60029	1	PHASE LOCK (A11J1) to SAMPLER-R (A4)
W9	F		8120-5021	1	FRAC-N DIGITAL (A14J1) to PULSE GENERATOR (A7)
W10	F		08753-60029	1	FRAC-N DIGITAL (A14J2) to REFERENCE (A12J1)
W11	F		08753-60029	1	FRAC-N DIGITAL (A14J3) to FRAC-N ANALOG (A13J1)
W12	F		08753-60029	1	FRAC-N ANALOG (A13J2) to REFERENCE (A12J2)
W13	F		08753-60026	1	REFERENCE (A12J3) to RP (EXT REF)
W24	SR		08753-20291	1	SOURCE ASSY (A3) to FP (R CHANNEL OUT)
W26	F		8120-5026	1	SOURCE ASSY (A3) to REFERENCE (A12J4)
W21	14R		8120-6876	1	MOTHERBOARD (A17J12) to REAR PANEL VGA OUT
W20	34R		8120-6880	1	MOTHERBOARD (A17J11) to CPU (A8J5)

* *n*W Wire Bundle (*n* is the number of wires in the bundle)
n Ribbon Cable (*n* is the number of wires in the ribbon)
F Flexible Coax Cable
SR Semi-Rigid Coax Cable


W21
A15W1
1
W13
W26
W20
W12
W1
W24
W11
W10
A6
A5
A4
W4
W3
W2
W9
W5
W8
W6
W7

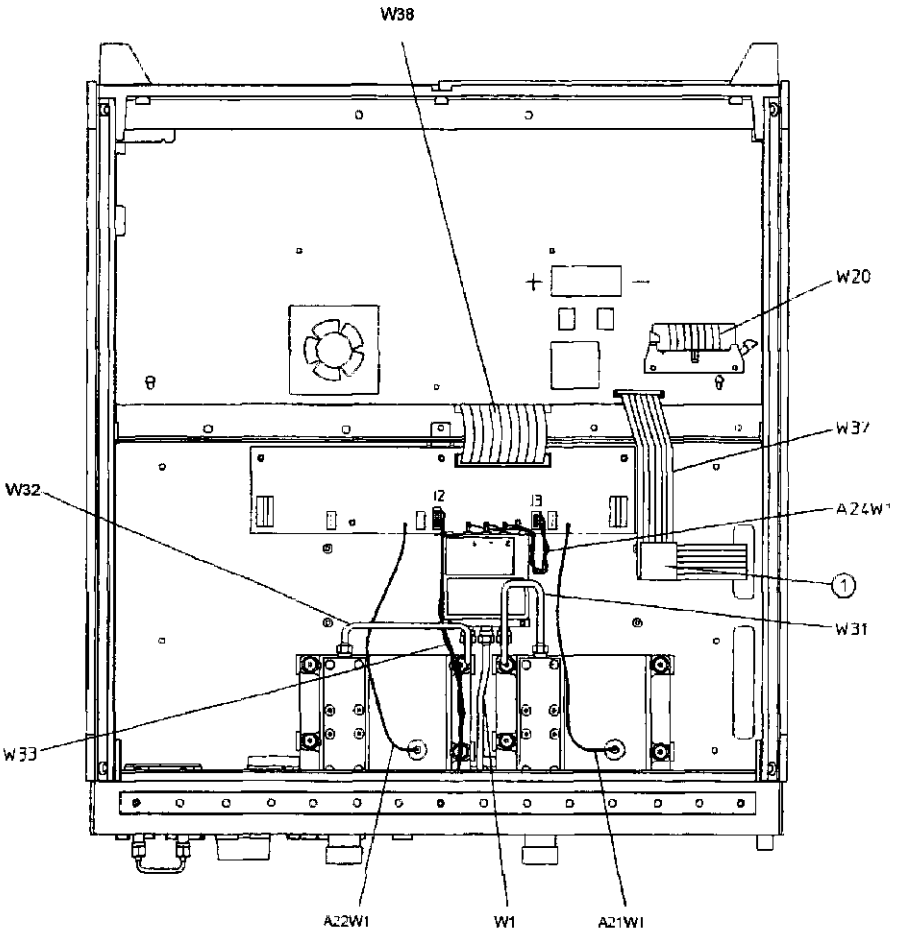
sg656e

Cables, Bottom

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
1			1400-0611	1	CABLE CLAMP
A21W1	1W		8120-6483	1	BLUE WIRE-TEST PORT 1 COUPLER (A21) to TEST SET INTERFACE (A25TP1)
A22W1	1W		8120-6483	1	GRAY WIRE-TEST PORT 2 COUPLER (A22) to TEST SET INTERFACE (A25TP2)
A24W1	3W		85047-60004	1	TRANSFER SWITCH (A24) to TEST SET INTERFACE (A25J3)
W1	8R		08753-20285	1	SOURCE ASSY (A3W4) to TRANSFER SWITCH (A24)
W20	34R		8120-6890	1	CPU/PIG (A9J7) to MOTHERBOARD (A17J11)
W31	8R		08753-20101	1	TEST PORT 1 COUPLER (A21) to TRANSFER SWITCH (A24)
W32	8R		08753-20102	1	TEST PORT 2 COUPLER (A22) to TRANSFER SWITCH (A24)
W33	4W		08753-60221	1	LED (A23J1) to TEST SET INTERFACE (A25J2)
W37	26R		8120-8670	1	DISK DRIVE (A20) to CPU/PIG (A9J8)
W38	40R		8120-6882	1	TEST SET INTERFACE (A25J1) to MOTHERBOARD (A17J2)

* *n*W Wire Bundle (*n* is the number of wires in the bundle)
*n*R Ribbon Cable (*n* is the number of wires in the ribbon)
SR Semi-Rigid Coax Cable

Cables, Bottom

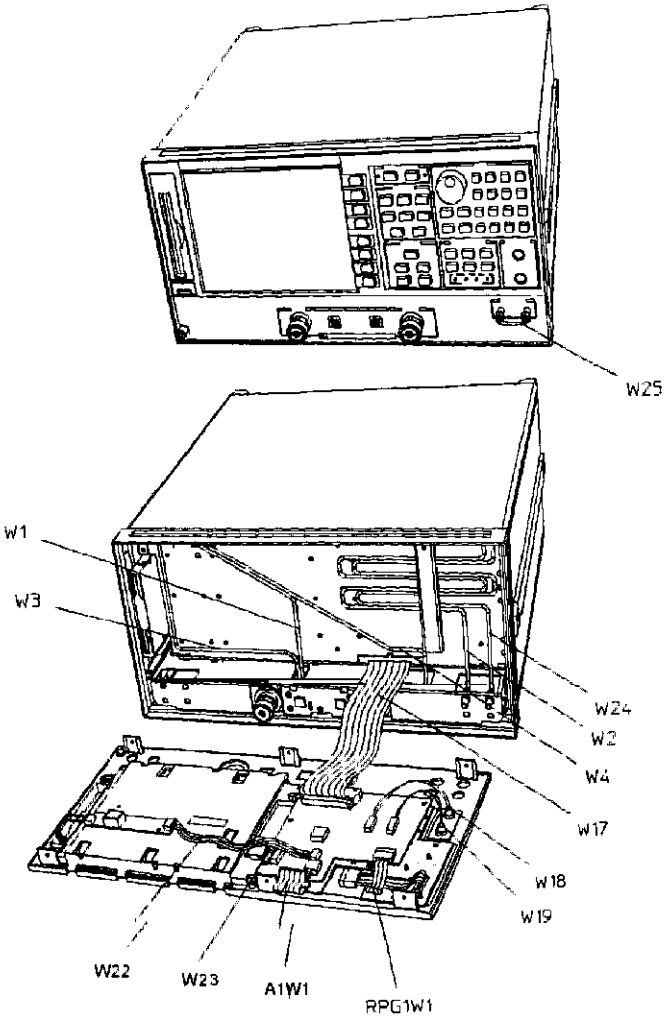


Cables, Front

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
A1W1	30R		8120-8439	1	FP KEYBOARD (A1J1) to FP INTERFACE (A2J2)
RPG1W1	5R		(part of RPG1)	1	RPG to FP INTERFACE (A2J5)
W1	SR		08753-20285	1	SOURCE ASSY (A3W4) to TRANSFER SWITCH (A24)
W2	SR		08753-20291	1	FP (R CHANNEL IN) to SAMPLER-R (A4)
W3	SR		08753-20286	1	TEST PORT 1 COUPLER (A21) to SAMPLER-A (A5)
W4	SR		08753-20287	1	TEST PORT 2 COUPLER (A22) to SAMPLER-B (A6)
W17	60R		8120-8431	1	FP INTERFACE (A2J1) to MOTHERBOARD (A17J1)
W18	3W		08711-60037	1	FP INTERFACE (A2J4) to FP (PROBE POWER)
W19	3W		08711-60037	1	FP INTERFACE (A2J3) to FP (PROBE POWER)
W22	5R		8120-8408	1	FP INTERFACE (A2J7) to INVERTER (A27)
W23	31R		8120-8409	1	FP INTERFACE (A2J6) to DISPLAY (A18)
W24	SR		08753-20220	1	SOURCE ASSY (A3) to FP (R CHANNEL OUT)
W25	SR		08720-20098	1	FP (R CHANNEL OUT) to FP (R CHANNEL IN)

* *n*W Wire Bundle (*n* is the number of wires in the bundle)
*n*R Ribbon Cable (*n* is the number of wires in the ribbon)
SR Semi-Rigid Coax Cable

Cables, Front

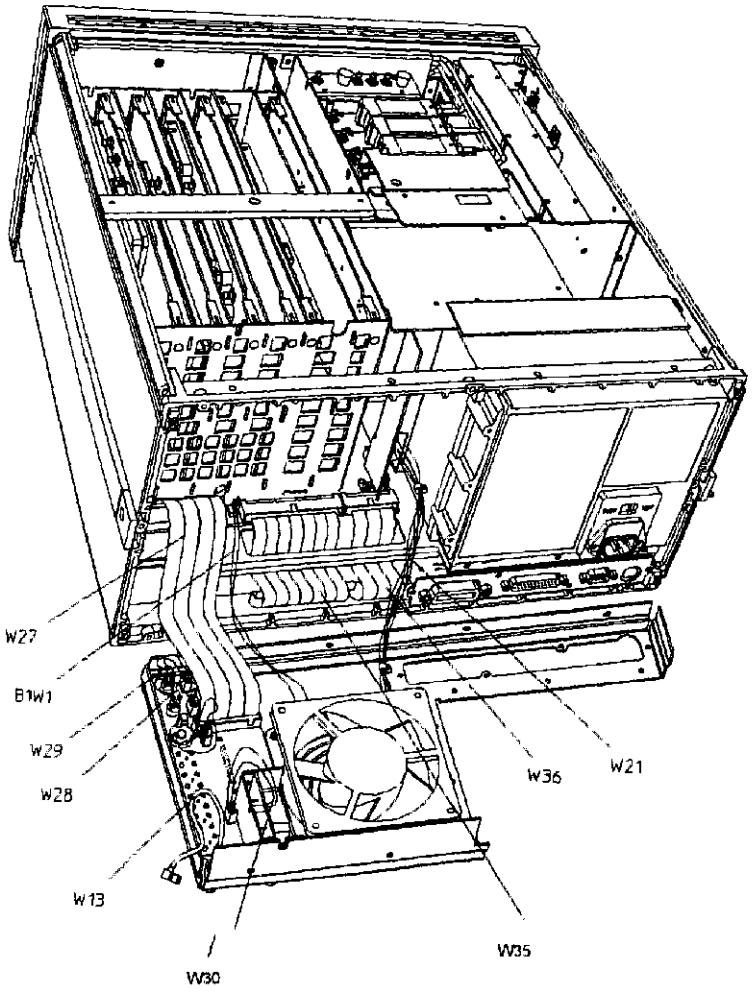


Cables, Rear

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
B1W1	2W		(part of B1)	1	FAN (B1) to MOTHERBOARD (A17J5)
W13	F		08753-60026	1	REFERENCE (A12J3) to RP (EXT REF)
W21	14R		8120-6876	1	MOTHERBOARD (A17J12) to RP (VGA OUT)
W27	34R		8120-6407	1	RP INTERFACE (A16J4) to MOTHERBOARD (A17J6)
W28	2W		86047-60005	1	RP INTERFACE (A16J10) to RP (PORT 1 FUSE)
W29	2W		85047-60005	1	RP INTERFACE (A16J11) to RP (PORT 2 FUSE)
W30	3W	1D5	8120-6458	1	RP INTERFACE (A16J3) to HIGH-STABILITY FREQ REF (A26J1)
W35	50R		8120-6379	1	CPU/PIG (A9J1) to MOTHERBOARD (A17J7)
W36	26R		8120-6382	1	CPU/PIG (A9J2) to MOTHERBOARD (A17J8)

* *n*W Wire Bundle (*n* is the number of wires in the bundle)
*n*R Ribbon Cable (*n* is the number of wires in the ribbon)
F Flexible Coax Cable

Cables, Rear



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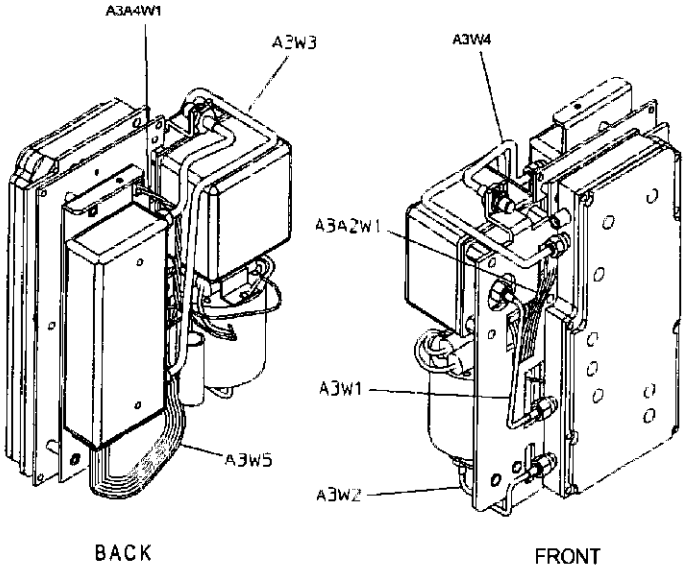
Cables, Source

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
A3A2W1	10R		08753-60034	1	EYO (A3A3) to ALC (A3A2J3)
A3A4W1	4W		08753-60035	1	CAVITY OSC (A3A4) to ALC (A3A2J2)
A3W1	SR		08753-20107	1	EYO (A3A3) to SOURCE ASSY (A3)
A3W2	SR		08753-20032	1	CAVITY OSC (A3A4) to SOURCE ASSY (A3)
A3W3	SR		08753-20106	1	SOURCE ASSY (A3) to ATTENUATOR (A3A5)
A3W4	SR		08753-20111	1	ATTENUATOR (A3A5) to W1
A3W5	10R		5062-0701	1	ALC (A3A2J1) to ATTENUATOR (A3A5)

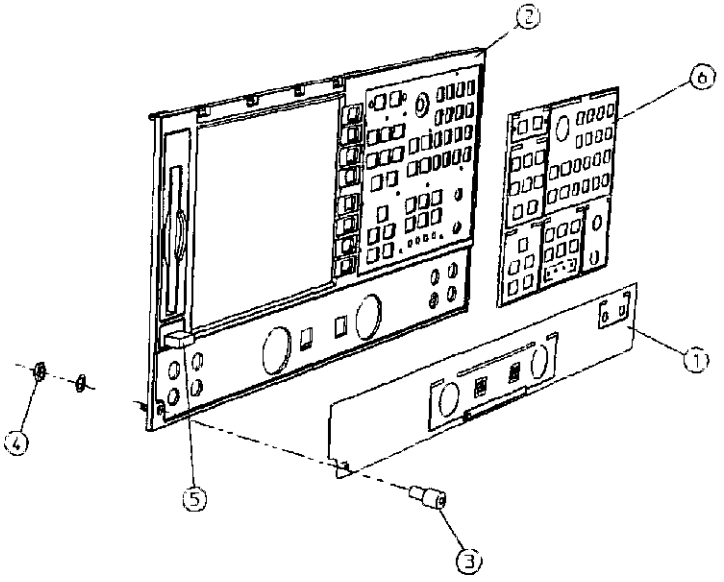
* *n*W Wire Bundle (*n* is the number of wires in the bundle)
*n*R Ribbon Cable (*n* is the number of wires in the ribbon)
SR Semi-Rigid Coax Cable


A3A4W1
A3W3
A3W4
A3A2W1
A3W1
A3W5
A3W2
BACK
FRONT
sg662e

Front Panel Assembly, Outside

Ref. Desig.	Option	HP Part Number	Qty	Description
1	STD	08753-80168	1	LOWER FRONT PANEL
1	075	08753-80170	1	LOWER FRONT PANEL
2		08753-20300	1	FRONT PANEL
3		1510-0038	1	GROUND POST
4		2950-0006	1	NUT HEX 1/4-32
4		2190-0067	1	WASHER LK .256 ID
5		08753-40015	1	LINE BUTTON
6		08753-80167	1	OVERLAY, UPPER FRONT PANEL

Front Panel Assembly, Outside



sgp63e

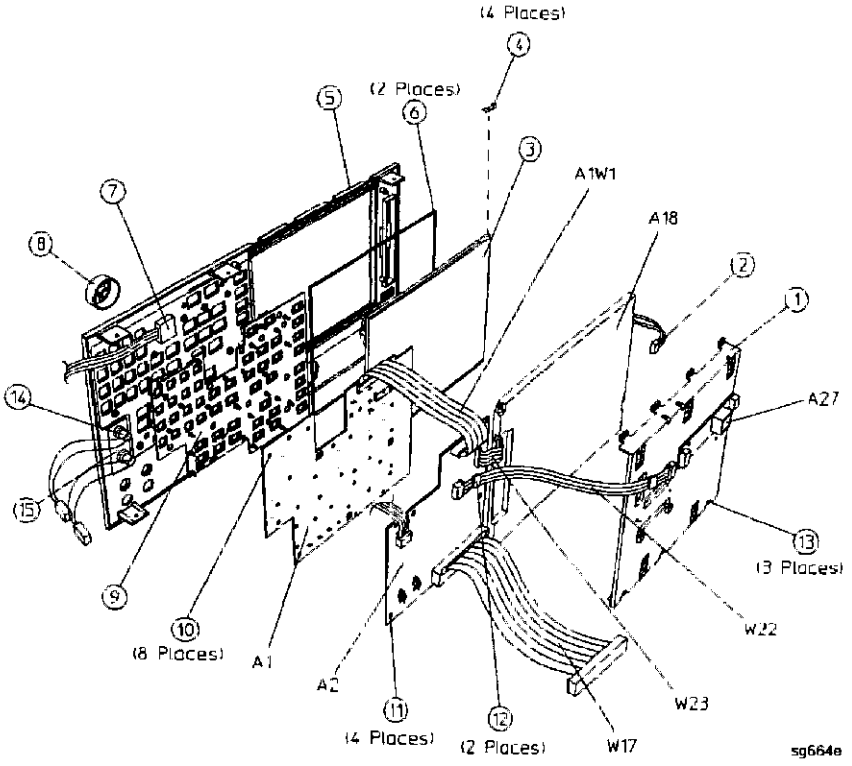
Front Panel Assembly, Inside

Ref. Desig.	Type	Opt	HP Part Number	Qty	Description
1			08720-40012	1	DISPLAY HOLD DOWN
2			2090-0566	1	DISPLAY LAMP
A18			08753-60325	1	LCD REPLACEMENT ASSY
3			1000-0995	1	DISPLAY GLASS
4			08720-00094	4	GROUNDING CLIPS
		1DT	08753-00135	1	FILLER PLCATE (*1)
5			08753-20300	1	FRONT PANEL
6			08720-00096	2	GASKET
7			1990-1864	1	RPG (INCLUDES CABLE AND HARDWARE)
8			E4400-40003	1	RPG KNOB
9			08720-40010	1	FLUBBER KEYPAD
10			0515-0430	8	SCREW SM 3.0 6CWPNTX
11			0515-0665	4	SCREW SMM 3.0 14CWPNTX
12			1400-1439	2	CABLE CLIP (*2)
13			0616-1960	3	SCREW SMM 3.0 8CWPNTX
14			08711-60037	2	CABLE ASSY, PROBE POWER
14			2950-0144	2	NUT, HEX 3/8-32
15			08711-00112	1	PLATE, PROBE POWER
A1			08720-60127	1	BD ASSY-FRONT PANEL
A2			08753-60311	1	BD ASSY-FRONT PANEL INTERFACE
A1W1	26R		8120-8439	1	A1 TO A2
A27			0950-3068	1	ASSY-INVERTER
W17	50R		8120-8431	1	A2 TO A17
W22	6R		8120-8408	1	CABLE-FP INTF (A2J7) to INVERTER (A27)
W23	31R		8120-8409	1	CABLE-FP INTF (A2J6) to DISPLAY (A18)

*1 Not shown. Replaces A18 and display glass for Option 1DT. Order new grounding clips when replacing filler plate.

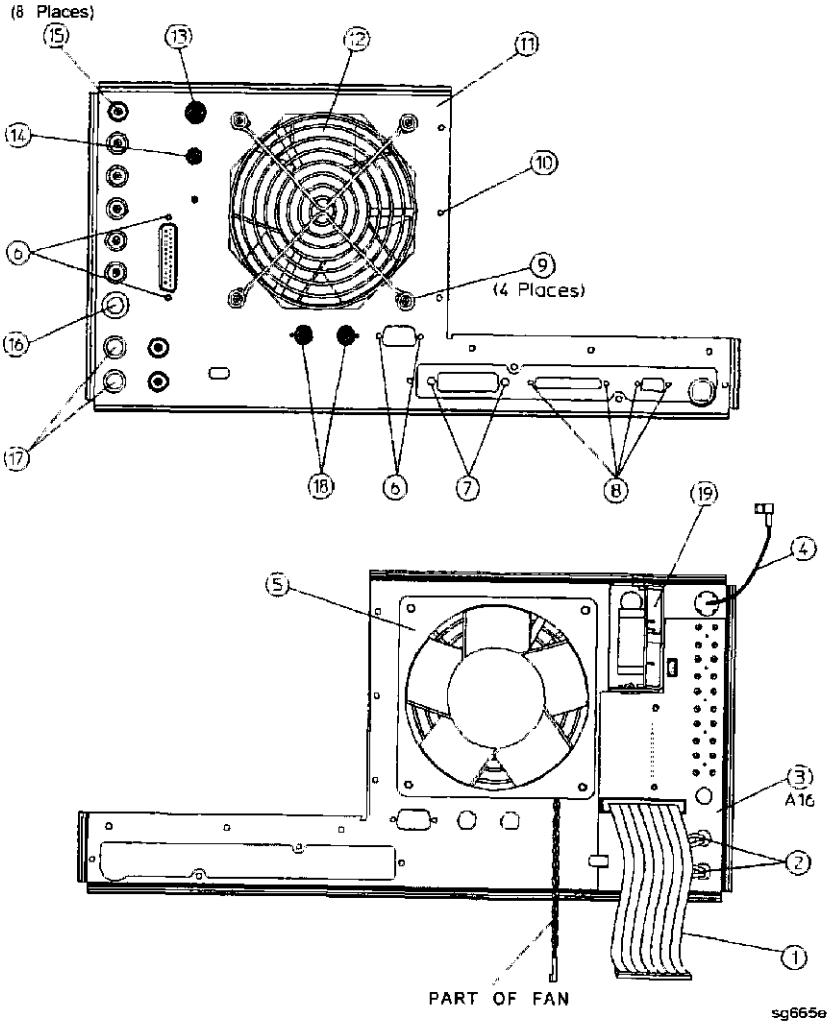
*2 Order with A2 and LCD hold down

Front Panel Assembly, Inside



Rear Panel Assembly

Ref. Desig.	Type	Opt	HP Part Number	Qty	Description
1	34R		8120-6407	1	RP INTERFACE (A16J4) TO MB (A17J6) (W27)
2			85047-60005	2	FUSE HARNESS ASSEMBLY
3 (A16)			08720-60138	1	BD ASSY-REAR PANEL INTERFACE (A16)
4			08753-60026	1	ASSY-EXTERNAL REFERENCE CABLE (W13)
5			08415-60036	1	ASSY-FAN
6			1251-2942	4	FASTENER CONN RP LOCK
7			2190-0034	2	WASHER LK .194ID 10
7			0380-0644	2	NUT STDF .327L 6-32
8			1251-7812	4	FASTENER CONN RP LOCK
9			0515-0379	4	SCREW SMM3.5x16 CWPNTX
9			3050-1192	4	FLAT WASHER
10			0515-0372	10	SCREWSMM3.0X8 CWPNTX
11			08720-00071	1	REAR PANEL SHEET METAL
12			3160-0281	1	FAN GUARD
13			6960-0419	1	HOLE PLUG
14			6960-0086	1	HOLE PLUG
15			2190-0102	8	WASHER LK .472ID
15			2950-0035	8	NUT HEX 15/32-32
16			0400-0271	1	GROMMET SN.5-515ID
17			2110-0047	2	FUSE
17			1400-0112	2	FUSE CAP
18			6960-0027	2	HOLE PLUGS
19		1D5			(see "Rear Panel Assembly, Option 1D5")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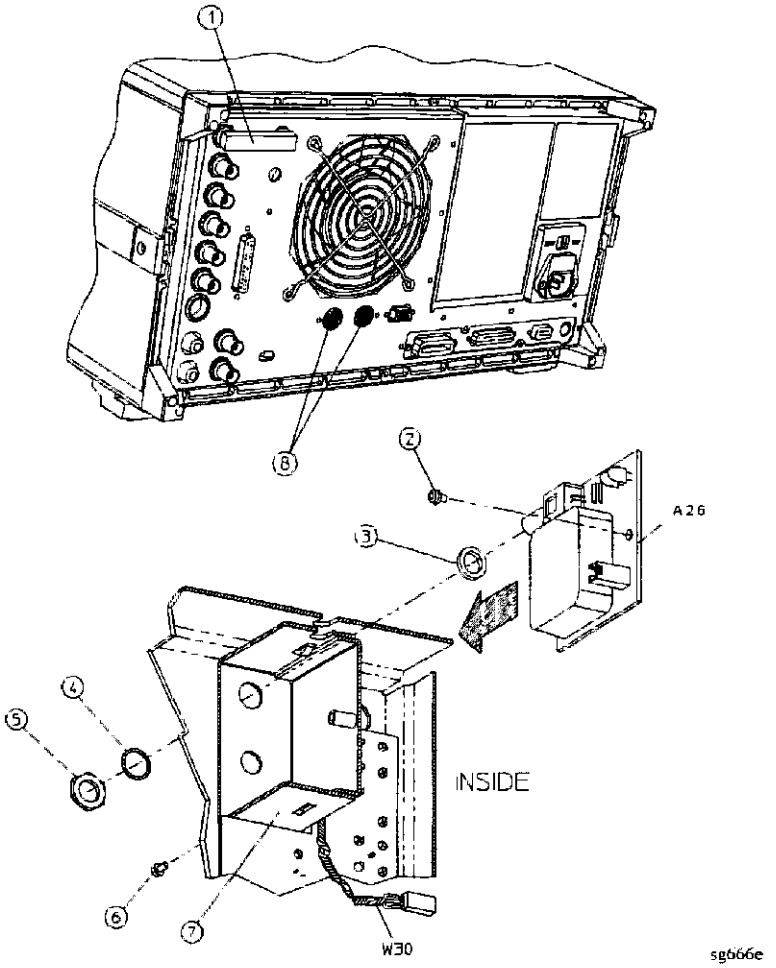
Rear Panel Assembly, Option 1D5

Ref. Desig.	Option	HP Part Number	Qty	Description
1	1D5	1250-1859	1	ADAPTER-COAX
2	1D5	0515-0374	1	SCREW-MACHINE M3.0x 10 CW-PN-TX
3	1D5	3050-1546	1	WASHER-FLAT .505ID NY
4	1D5	2190-0068	1	WASHER-LOCK .505ID
5	1D5	2950-0054	1	NUT-SPECIALTY 1/2-28
6	1D5	0515-0430	1	SCREW-MACHINE M3.0x 6 CW-PN-TX
7	1D5	08753-00078	1	BRACKET-OSC BD
8		6960-0027	2	HOLE PLUGS
A26	1D5	08753-60158	1	BD ASSY-HIGH STABILITY FREQ REF
W30	1D5	8120-6458	1	RP INTERFACE (A16J3) to HIGH-STABILITY FREQ REF (A26J1)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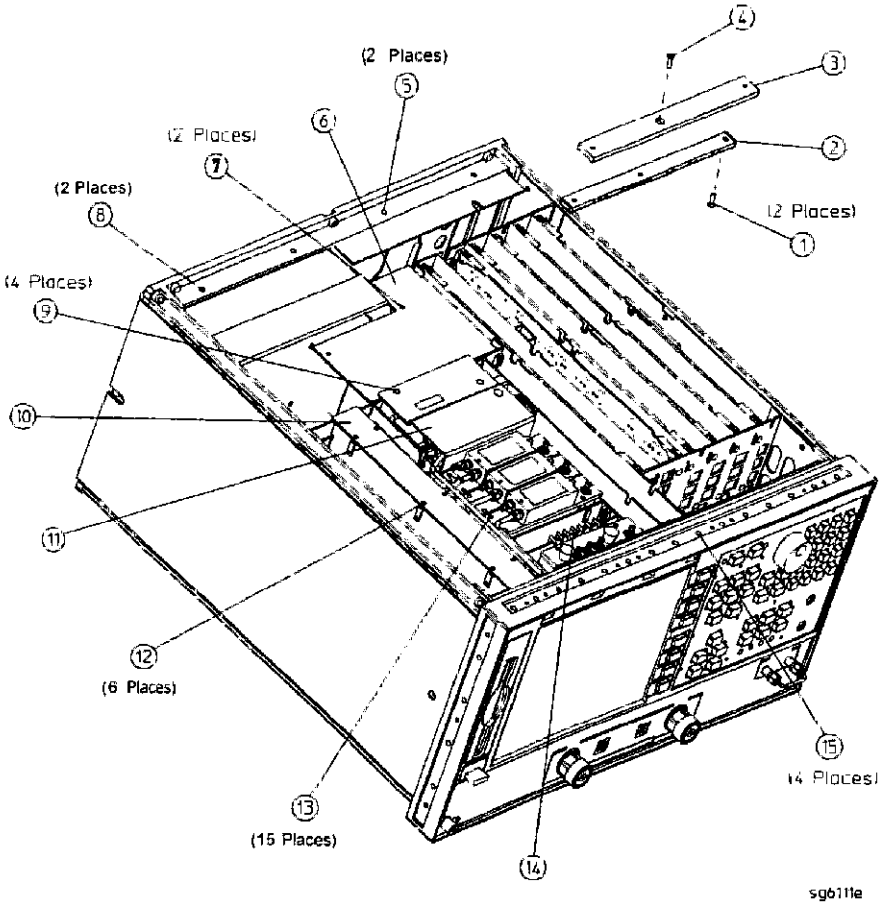
Hardware, Top

Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-2799	2	SCREW-MACHINE M3.0x10 CW-FL-TX
2		08753-40014	1	STABILIZER-PC BOARD
3		08753-20062	1	STABILIZER CAP
4		0515-2036	1	SCREW-MACHINE M3.0x16 PC-FL-TX
5		0515-0458	2	SCREW-MACHINE M3.5x8 CW-PN-TX
6		08753-00107	1	AIR FLOW COVER
7		0515-0374	2	SCREW-MACHINE M3.0x 10 CW-PN-TX
8		0515-0377	2	SCREW-MACHINE M3.5x10 CW-PN-TX
9		0515-0374	2	SCREW-MACHINE M3.0x12 CW-PN-TX
10		08753-00129	1	GSP COVER
11		08753-00113	1	BRACKET-SOURCE (SOURCE STRAP)
12		0515-0374	6	SCREW-MACHINE M3.0x10 CW-PN-TX
13		0515-0374	15	SCREW-MACHINE M3.0x10 CW-PN-TX
14		08753-00040	1	CLIP-PUISERGROUND
16		0515-1400	3	SCREW-MACHINE M3.5x8 PC-FL-TX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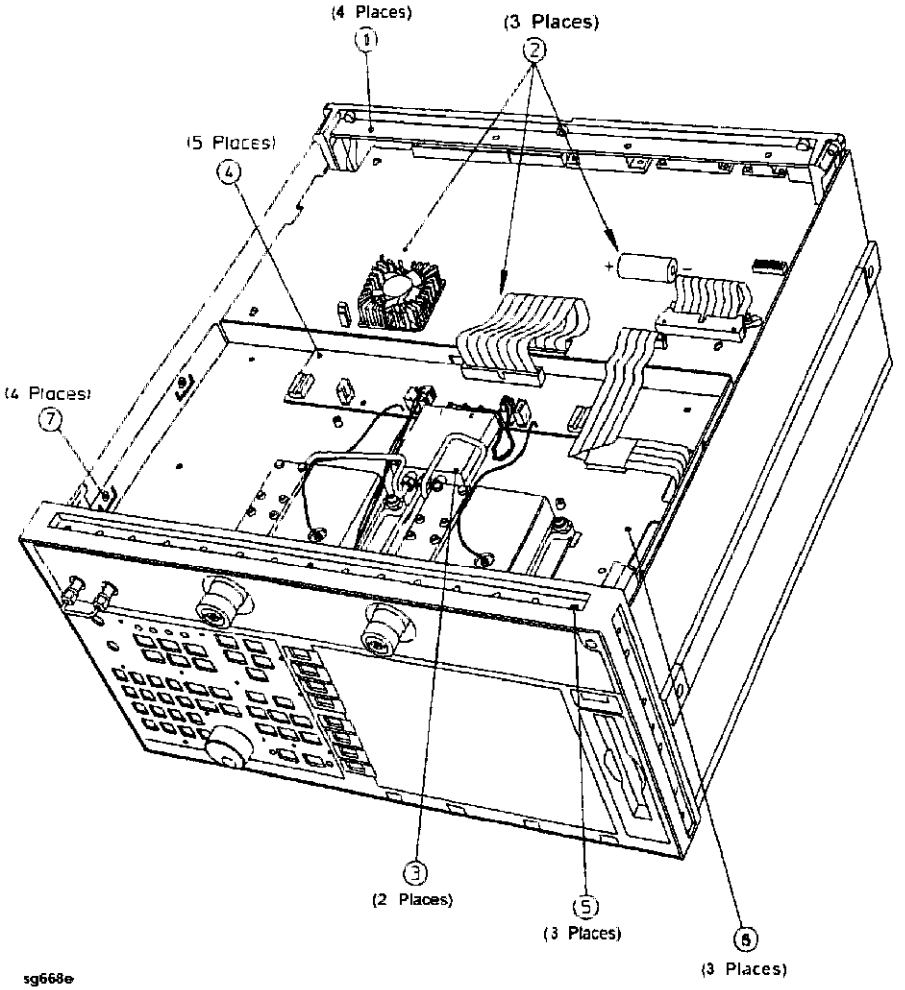
Hardware, Bottom

Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-0458	4	SCREW-MACHINE M3.5X8 CW-PN-TX
2		0515-0430	3	SCREW-MACHINE M3.0x6 CW-PN-TX
3		0515-0667	2	SCREW-MACHINE M3.0x25 CW-PN-TX
4		0515-0430	5	SCREW-MACHINE M3.0x6 CW-PN-TX
5		0515-1400	3	SCREW-MACHINE M3.5x8 PC-FL-TX
6		0515-0875	8	SCREW-MACHINE M3.0x16 CW-PN-TX
7		0515-0458	4	SCREW-MACHINE M3.0x16 CW-PN-TX

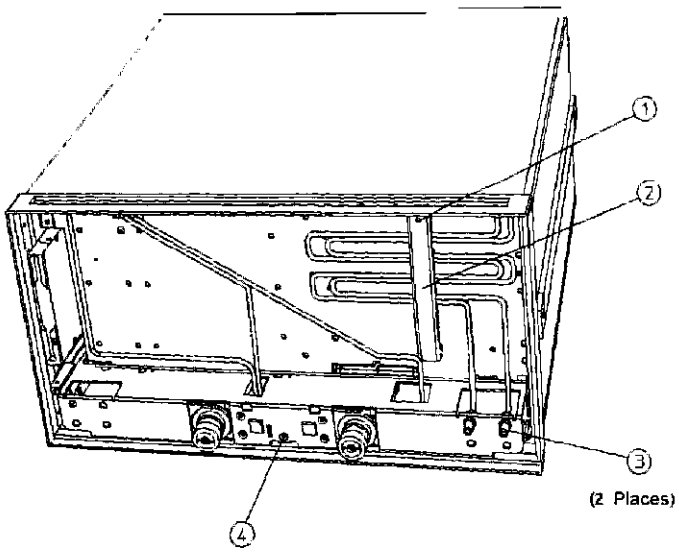
Hardware, Bottom



Hardware, Front

Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-0665	1	SMM 3.0x14 CWPNTX
2		08753-00137	1	BRACKET-CABLE SUPPORT
3		1250-1251	2	ADAPTER FEMALE SMA/FEMALE SMA
4		0515-1946	1	SCREW-MACHINE M3.0x6 PC-FL-TX

Hardware, Front



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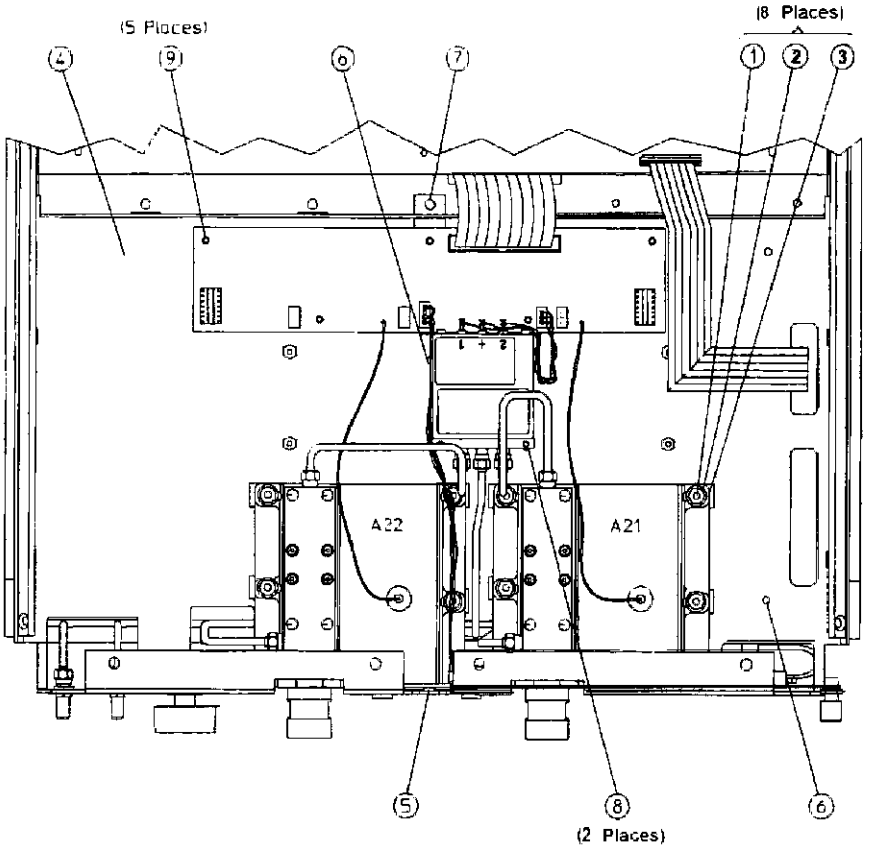
Hardware, Test Set Deck

Ref. Desig.	Option	HP Part Number	Qty	Description
1		08753-20296	8	SHOULDER SCREW
2		08753-40013	8	GUIDE WASHER
3		08753-20293	8	PRESSURE SPRING
4		08753-00127	1	CHASSIS-TEXT SET
5		0515-1946	1	SCREW-MACHINE M3.0x6 PC-FL-TX
6		0515-0375	2	SCREW-MACHINE M3.0x16 CW-PN-TX
7		0515-0430	1	SCREW-MACHINE M3.0x6 CW-PN-TX
8		0515-0667	2	SCREW-MACHINE M3.0x25 CW-PN-TX
9		0515-0430	6	SCREW-MACHINE M3.0x6 CW-PN-TX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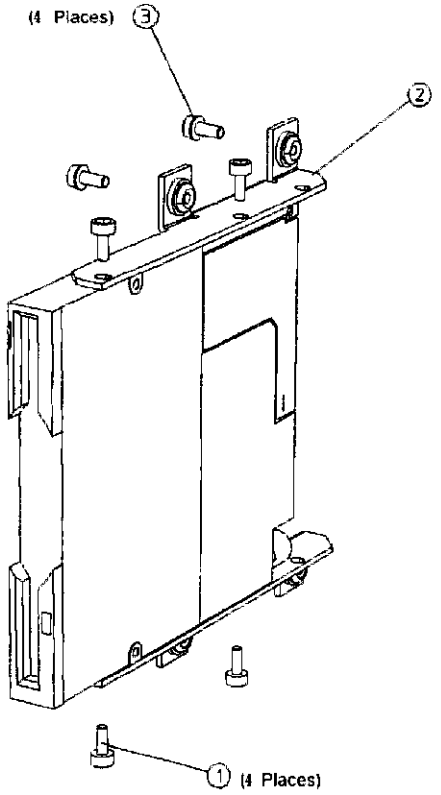
Hardware, Disk Drive Support

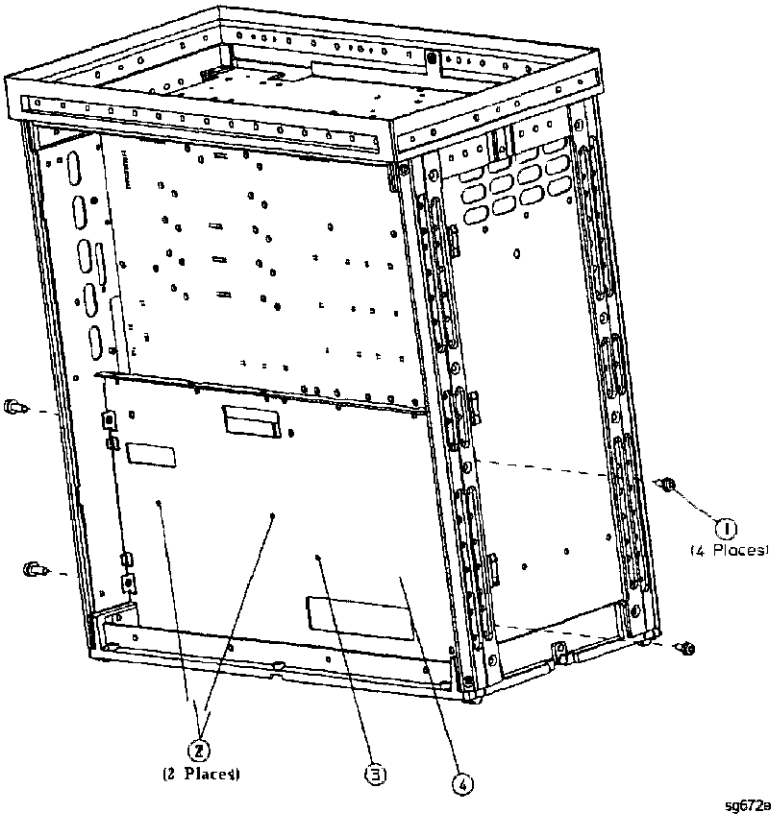
Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-1048	4	SCREW-M 2.5X4 SOCKET HEAD, HEX.
2		08720-00021	1	DISK DRIVE BRACKET
3		0515-0374	4	SCREWS -MACHINE M 3.0X10 CWPNTX



sg671e

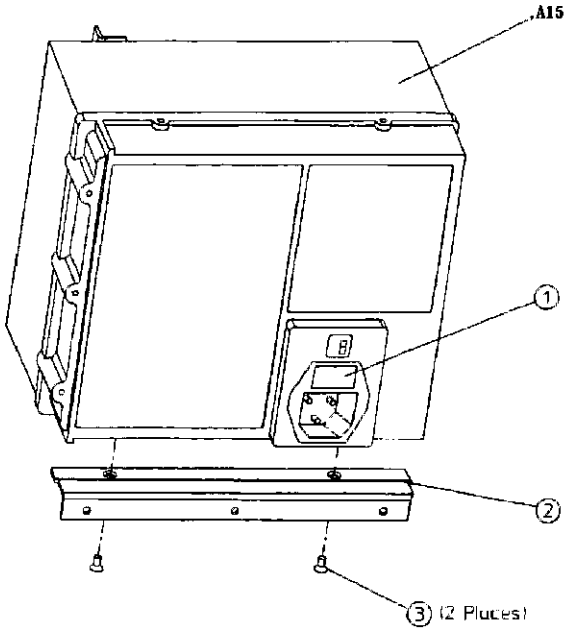
Hardware, Memory Deck

Ref. Desig.	Option	HP Part Number	Qty	Description
1		0515-0458	4	SCREW-MACHINE M3.5x8 CW-PN-TX
2		0515-0430	2	SCREW-MACHINE M3.0x6 CW-PN-TX
3		0515-0376	1	SCREW-MACHINE M3.0x14 CW-PN-TX
4		08753-00128	1	DECK-MEMORY



Hardware, Preregulator

Ref. Desig.	Option	HP Part Number	Qty	Description
1		2110-0780	1	FUSE 3A 250V NON-TIME DELAY (CSA/UL)
1		2110-0655	1	FUSE 3.15A 250V NON-TIME DELAY (IEC)
2		08753-40066	1	BRACKET-PREREGULATOR
3		0515-1400	2	SCREW-MACHINE M3.5x8 CW-FL-TX
A15		08753-60098	1	PREREGULATOR-ASSY
A15		08753-69098	1	PREREGULATOR-ASSY (REBUILT-EXCHANGE)



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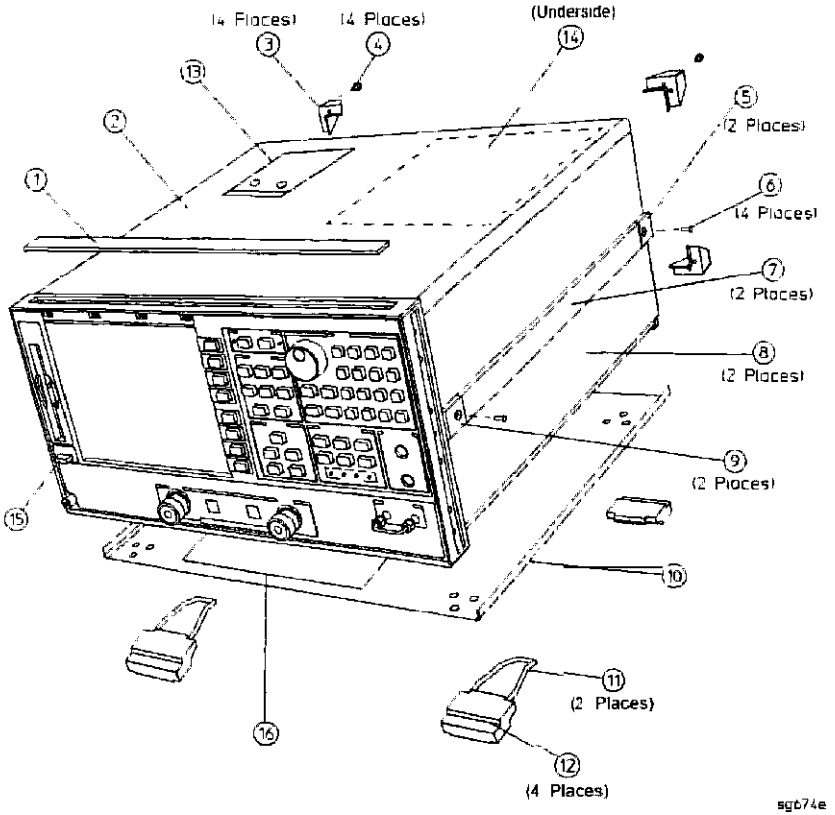
Hardware, Preregulator

Chassis Parts, Outside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		5041-9176	1	TRIMSTRIP
2		08720-00078	1	COVER-TOP
3		5041-9188	4	REAR STANDOFF
4		0515-1402	4	SCREW SMM 3.5 8 PCPNTX
5		5041-9187	2	REAR CAP-SIDE STRAP
6		0515-1384	4	SCREW SMM 5.0 10 PCFLTX
7		08720-00081	2	SIDE STRAP
8		08720-00080	2	COVER-SIDE
9		5041-9186	2	FRONT CAP-SIDE STRAP
10		08720-00079	2	COVER-BOTTOM
11		1460-1345	2	FOOT ELEVATOR
12		5041-9167	4	FOOT
13		08753-80066	1	LABEL: CAUTION WARNING
14		08753-80174	1	LABEL: LOCATION DIAGRAM
15		08753-40015	1	LINE BUTTON
16		5180-8500	1	MYLAR INSULATOR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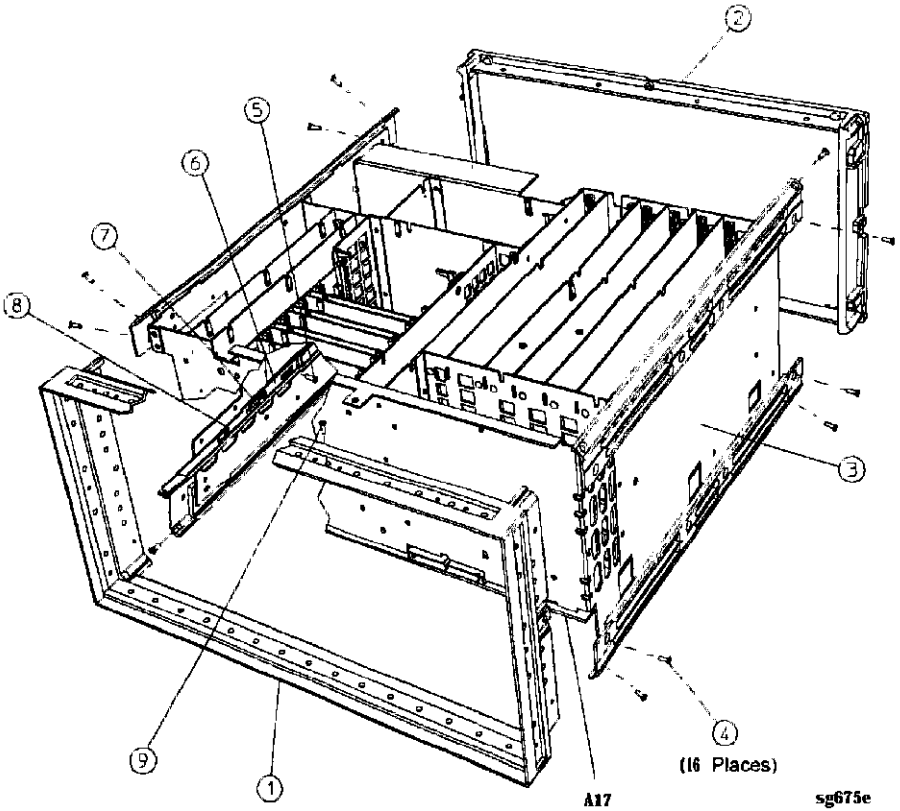
Chassis Parts, Inside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		5022-1190	1	FRONT PANEL FRAME
2		5021-5808	1	REAR FRAME
3		08753-60314	1	ASSY-CARDCAGE/MOTHER
4		0515-2086	16	SCREW SMM4.0x7 PCFLTX
5		0515-0430	1	SCREW M3.0x 6 CWPNTX*
6		08720-00083	1	INSULATOR SWITCH*
7		1460-1673	1	SPRING EXTENSION .138 OD
8		08720-00077	1	SWITCH ROD*
9		0515-1400	1	SMM 3.5x8 PCFLTX
A17		08753-60270	1	BD ASSY-MOTHERBOARD

* Part of CARDCAGE/MOTHER assembly (item 3).

Chassis Parts, Inside



Miscellaneous

Description	HP Part Number
Service Tools	
HP 8753 TOOL KIT *includes the following:*	08753-60023
RF CABLE-INPUT R	08753-20028
EXTENDER BOARD ASSEMBLY-RECEIVER	08753-60019
EXTENDER BOARD ASSEMBLY-SOURCE	08753-60020
EXTENDER BOARD ASSEMBLY-CARD CAGE	08753-60155
ADAPTER-MALE SMB TO MALE SMB	1250-0669
ADAPTER-MALE TYPE N TO FEMALE SMA	1250-1250
CABLE ASSEMBLY	5061-1022
BAG-ANTISTATIC 13×15	9222-1132
Documentation	
HP 8753E EXAMPLE PROGRAM DISK #1	08753-10028
HP 8753E EXAMPLE PROGRAM DISK #2	08753-10029
HP 8753E SERVICE GUIDE	08753-90374
HP 8753E OPTION 011 SERVICE GUIDE	08753-90404
HP 8753E MANUAL SET *includes the following*	08753-90365
HP 8753E HP-IB PROGRAMMING AND COMMAND REFERENCE GUIDE	08753-90366
HP 8753E HP BASIC PROGRAMMING EXAMPLES GUIDE	08753-90413
HP 8753E USER'S GUIDE *(includes Quick Reference, 08753-90368)*	08753-90367
HP 8753E INSTALLATION/QUICK START GUIDE	08753-90369
HP 8753E SYSTEM VERIFICATION AND PERFORMANCE TESTS	08753-90394
HP 8753E OPTION 011 MANUAL SET *includes the following:*	08753-90370
HP 8753E HP-IB PROGRAMMING AND COMMAND REFERENCE GUIDE	08753-90366
HP 8753E HP BASIC PROGRAMMING EXAMPLES GUIDE	08753-90413
HP 8753E OPTION 011 USER' S GUIDE *(includes Quick Reference, 08753-90373)*	08753-90371
HP 8753E OPTION 011 INSTALLATION/QUICK START GUIDE	08753-90372
HP 8753E OPTION 011 SYSTEM VERIFICATION AND PERFORMANCE TESTS	08753-90305
Upgrade Kits	
HARMONIC MEASUREMENT UPGRADE KIT	8753EU OPT 002
6 GHz UPGRADE KIT FOR HP 8753E	8753EU OPT 006
6 GHz UPGRADE KIT FOR HP 8753E OPTION 011	8753EU OPT 611
TIME DOMAIN UPGRADE KIT	8753EU OPT 010
FIRMWARE UPGRADE KIT	8753EU OPT 099
HIGH-STABILITY FREQUENCY REFERENCE RETROFIT KIT	8753EU OPT 1D5

Description	HP Part Number
Protective Caps for Connectors	
FEMALE HP-IB CONNECTOR	1252-5007
FEMALE TEST SET I/O	1252-4690
FEMALE PARALLEL PORT	1252-4690
RS-232 CONNECTOR	1252-4697
7-mm TEST PORTS	1401-0249
FEMALE TYPE-N TEST PORTS (OPTIONS 011 AND 075)	1401-0247
Fuses used on the A8 Post Regulator	
FUSE 0.5A 125V NON-TIME DELAY 0.25x0.27	2110-0046
FUSE 0.75A 125V NON-TIME DELAY 0.26x0.27	2110-0424
FUSE 1A 125V NON-TIME DELAY 0.25x0.27	2110-0047
FUSE 2A 125V NON-TIME DELAY 0.25x0.27	2110-0425
FUSE 4A 125V NON-TIME DELAY 0.25x0.27	2110-0476
HP-IB Cables	
HP-IB CABLE, 1M (3.3 FT)	HP 10833A
HP-IB CABLE, 2M (6.6 FT)	HP 10833B
HP-IB CABLE 4M (13.2 FT)	HP 10833C
HP-IB CABLE, 0.5M (1.6 FT)	HP 10833D
ESD Supplies	
ADJUSTABLE ANTISTATIC WRIST STRAP	9300-1367
5 FT GROUNDING CORD *for wrist strap*	9300-0980
2 x 4 FT ANTISTATIC TABLE MAT WITH 15 FT GROUND WIRE	9300-0797
ANTISTATIC HEEL STRAP *for use on conductive floors*	9300-1126
Other	
HP 8763E KEYBOARD OVERLAY *for external keyboard*	08753-80131
RACKMOUNT KIT WITHOUT HANDLES	5062-3978
RACK MOUNT KIT WITH HANDLES	5062-4073
FRONT HANDLE	5062-3991
FLOPPY DISKS, 3.5 INCH DOUBLE-SIDED (box of 10)	HP 92192A

Table 13-1.
Reference Designations, Abbreviations, and Options

REFERENCE DESIGNATIONS	
A	assembly
B	fan; motor
J	electrical connector (stationary portion); jack
RPG	rotary pulse generator
W	cable; transmission path; wire

ABBREVIATIONS	
A	ampere
ALC	automatic level control
ASSY	assembly
AUX	auxiliary
BD	board
COAX	coaxial
CPU	central processing unit
CW	conical washer (screws)
D	diameter
ESD	electrostatic discharge
EXT	external
EYO	YIG oscillator
FL	flathead (screws)
FP	front panel
FRAC-N	fractional N
FREQ	frequency
GHz	gigahertz
HEX	hexagonal
HP	Hewlett-Packard
HP-IB	Hewlett-Packard interface bus
HX	hex recess (screws)
ID	inside diameter
IF	intermediate frequency
I/O	input/output
LED	light-emitting diode
M	meters
M	metric hardware
MHz	megahertz
mm	millimeters
MON	monitor
NOM	nominal
NY	nylon
OD	outside diameter
Opt	option
OSC	oscillator
PN	panhead
PC	patch lock (screws)
PC	printed circuit
PIG	peripheral interface group
PN	panhead (screws)
REF	reference
REPL	replacement
RP	rear panel
SH	socket head cap (screws)
TX	MRX recess (screws)
Qty	quantity
V	volt
WFR	wire formed
W/O	without
YIG	yttrium-iron garnet

OPTIONS	
002	harmonics measurement
006	6 GHz performance
010	time domain
011	w/o test set
075	75 ohm test set
1D5	10 MHz precision ref

14

Assembly Replacement and Post-Repair Procedures

This chapter contains procedures for removing and replacing the major assemblies of the HP 8753E network analyzer. A table showing the corresponding post-repair procedures for each replaced assembly is located at the end of this chapter.

Replacing an Assembly

The following steps show the sequence to replace an assembly in an HP 8753E Network Analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Warning These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.

Warning The opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.

Warning The power cord is connected to internal capacitors that may remain live for 10 seconds after disconnecting the plug from its power supply.

Caution Many of the assemblies in this instrument are very susceptible to damage from ESD (electrostatic discharge). Perform the following procedures only at a static-safe workstation and wear a grounding strap.

Procedures described in this chapter

The following pages describe assembly replacement procedures for the HP 8753E assemblies listed below:

- Line Fuse
- Covers
- Front Panel Assembly
- Front Panel Interface and Keypad Assemblies **(A1, A2)**
- Display Lamp and Assembly **(A18, A27)**
- Rear Panel Assembly
- Rear Panel Interface Board Assembly **(A16)**
- **A3** Source Assembly
- **A4, A5, A6** Samplers and **A7** Pulse Generator
- **A8, A10, A11, A12, A13, A14** Card Cage Boards
- **A9** CPU/PIG Board
- **A9BT1** Battery
- **A15** Preregulator
- **A17** Motherboard Assembly
- **A19** Graphics Processor
- **A20** Disk Drive
- **A21, A22** Test Port Couplers
- **A23** LED Board
- **A24** Transfer Switch
- **A25** Test Set Interface
- **A26** High Stability Frequency Reference (Option 1D5)
- **B1** Fan

Line Fuse

Tools Required

- small slot screwdriver

Removal

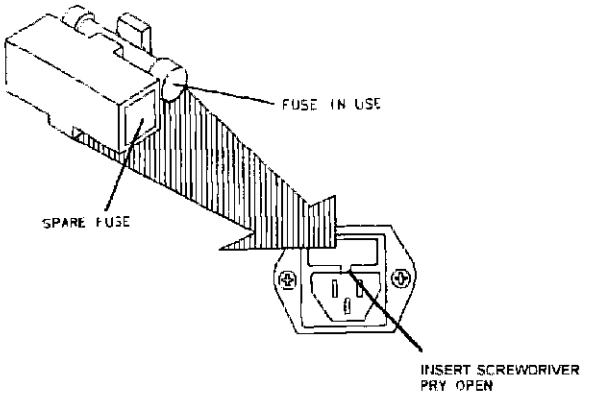
Warning **For continued protection against fire hazard, replace fuse only with same type and rating (3 A 250 V F). The use of other fuses or materials is prohibited.**

1. Disconnect the power cord.
2. Use a small slot screwdriver to pry open the fuse holder.
3. Replace the blown fuse with a 3 A 250 V F fuse (HP part number 2110-0708).

Replacement

1. Simply replace the fuse holder.

Line Fuse



qg652d

Covers

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- T-20 TORX screwdriver
- T-25 TORX screwdriver

Removing the top cover

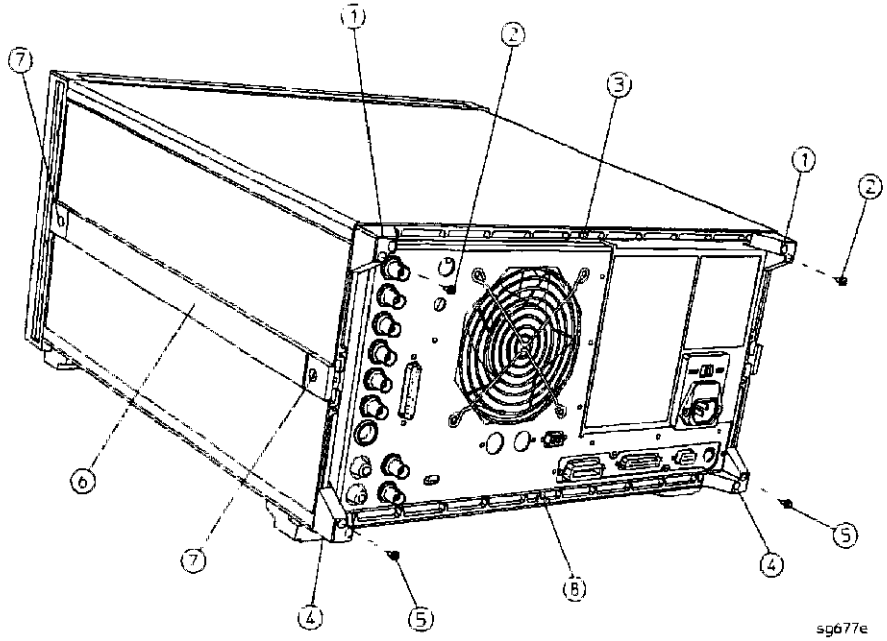
1. Remove both upper rear feet (item 1) by loosening the attaching screws (item 2).
2. Loosen the top cover screw (item 3).
3. Slide cover off.

Removing the side covers

1. Remove the top cover.
2. Remove the lower rear foot (item 4) that corresponds to the side cover you want to remove by loosening the attaching screw (item 5).
3. Remove the handle assembly (item 6) by loosening the attaching screws (item 7).
4. Slide cover off.

Removing the bottom cover

1. Remove both lower rear feet (item 4) by loosening the attaching screws (item 5).
2. Loosen the bottom cover screw (item 8).
3. Slide cover off.


1
2
3
7
1
2
6
7
4
5
8
4
5
sg677e

Front Panel Assembly

Tools Required

- T- 10 TORX screwdriver
- T- 15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

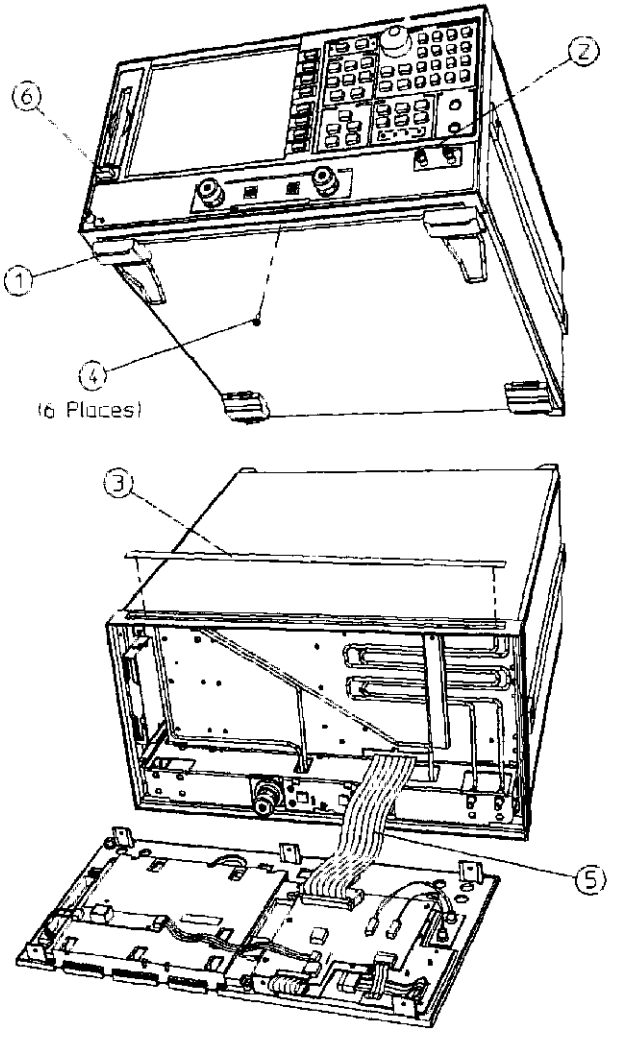
1. Disconnect the power cord.
2. Remove the front bottom feet [item 1).
3. Remove all of the RF cables that are attached to the front panel (item 2).
4. Remove the line button (item 6).
5. Remove the trim strip (item 3) from the top edge of the front frame by prying under the strip with a small slot screwdriver.
6. Remove the six screws (item 4) from the top and bottom edges of the frame.
7. Slide the front panel over the test port connectors.
8. Disconnect the ribbon cable (item 5). The front panel is now free from the instrument.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semirigid cables, it is recommended that the connections be torqued to 10 m-lb.

Front Panel Assembly



sg679e

Front Panel Interface and Keypad Assemblies (A1, A2)

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

1. Remove the front panel assembly from the analyzer (refer to "Front Panel Assembly" in this chapter).
2. Disconnect all cables from the front panel interface board (items 1, 2, 3, 4, 6, and 7).
   - Disconnect item 4 by pulling up on the corners of the connector base. This will release the cable for easy removal. *Damage may occur to the connector if this step is not followed*
   - Disconnect item 7 by sliding the ribbon cable away from its cable clamp.
3. Remove the four screws (item 5), attaching the interface board.
4. Remove the nine screws from the A1 front panel board to access and remove the keypad.

Replacement

1. Reverse the order of the removal procedure.

Caution Damage may result if the following step is not followed.

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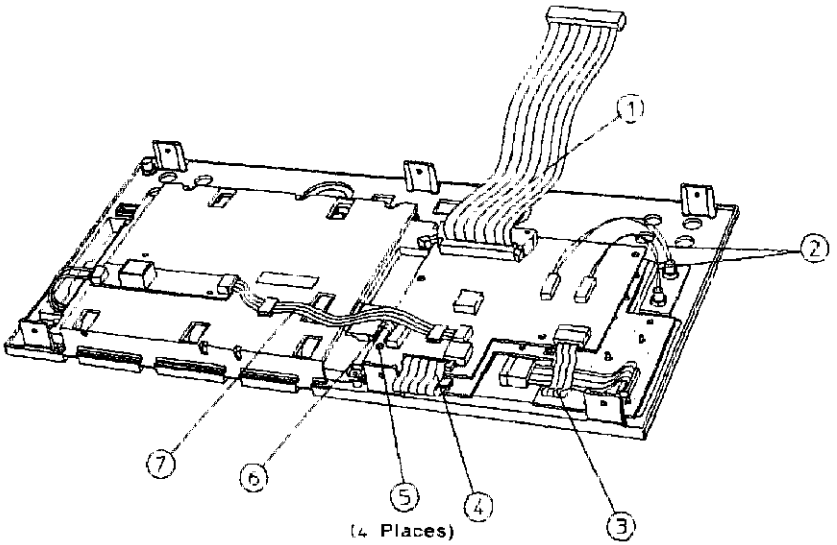
2. To reconnect item 7, ensure that the ribbon cable is placed squarely into both of its cable clamps.

Front Panel Interface and Keypad Assemblies



sg680e

Display Lamp and Assembly (A18, A27)

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

1. Remove the front panel assembly (refer to "Front Panel Assembly" in this chapter).
2. Disconnect the cables (items 2, 3 and 4) from the Al assembly.
3. Remove the three screws (item 1) that attach the mounting plate and display to the front panel.
4. Remove the mounting plate and the display from the front panel.

Note The bottom half of the following figure depicts the rear view of the A18 assembly with the mounting plate removed. Use the location of the display lamp cable (item 4) to aid in orientation.

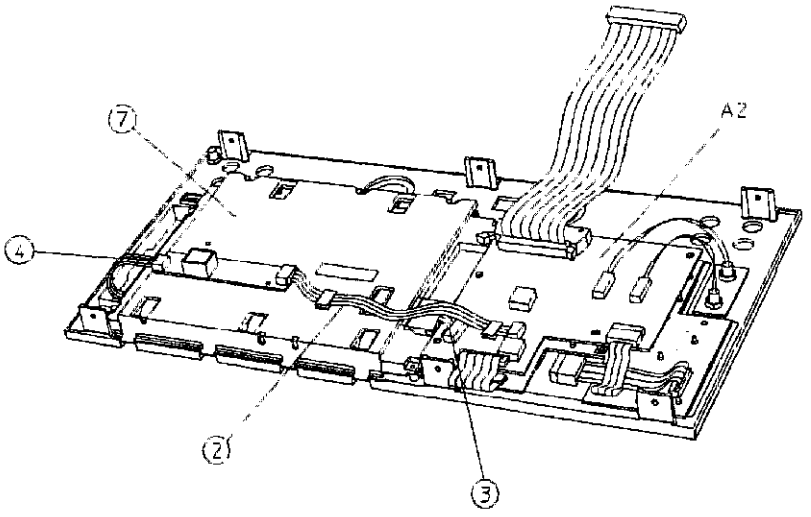
5. Remove the three screws (item 5) from the outside of the display.
6. Pull the lamp [item 6) out with a curving side motion, as shown.

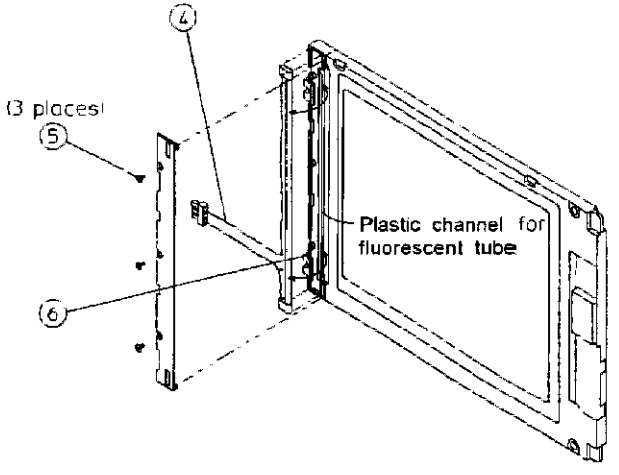
Replacement

1. Reverse the order of the removal procedure.
2. Be sure to route ribbon cable 2 through the cable clamp on the A2 assembly and the LCD mounting plate (item 7).

Caution Be sure that cables are plugged in square and correct. Failure to do so will result in serious component damage.

Display Lamp and Assembly





sg681e

Rear Panel Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

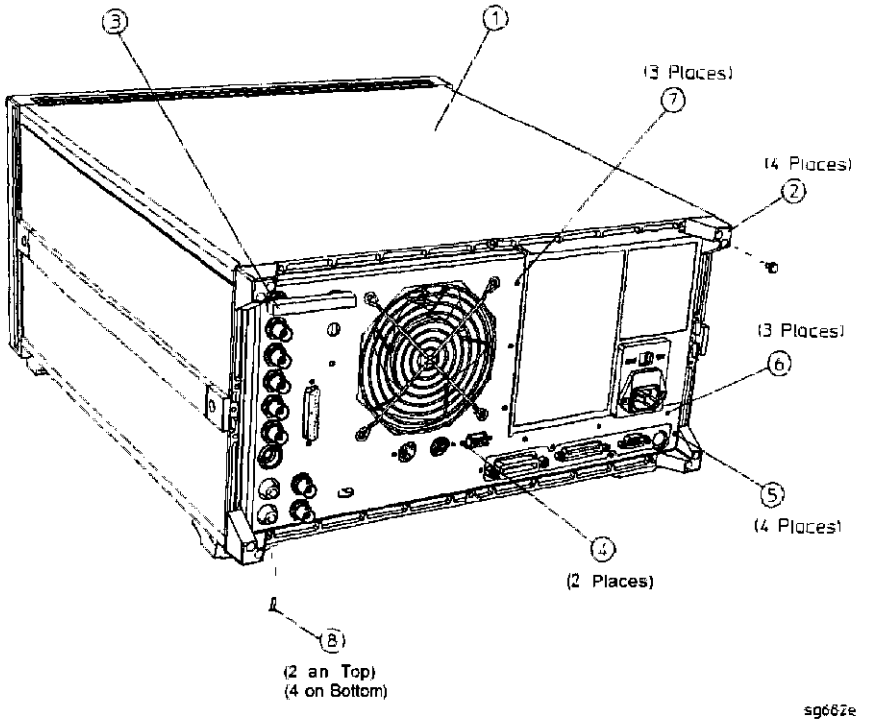
1. Disconnect the power cord and remove the top (item 1) and bottom covers (refer to "Covers" in this chapter).
2. Remove the four rear standoffs (item 2).
3. If the analyzer has option 1D5, remove the BNC jumper from the high stability frequency reference (item 3).
4. Remove the four screws (item 5) that attach the interface bracket to the rear panel.
5. Remove the six screws (item 6) and (item 7), that attach the preregulator to the rear panel.
6. Remove the six screws (item 8) from the rear frame: two from the top edge and four from the bottom edge.
7. Remove the screw from the pc (item 9) board stabilizer and remove the stabilizer.
8. Lift the reference board (A12) from its motherboard connector and disconnect the flexible RF cable from its connector on A12 (item 10)

   Identify the wiring harness leading to the VGA connector (item 4). Follow this harness back to its connection on the motherboard. The air flow cover, attached by two screws, will have to be removed to get to this connection. Disconnect the VGA wire harness at this point.

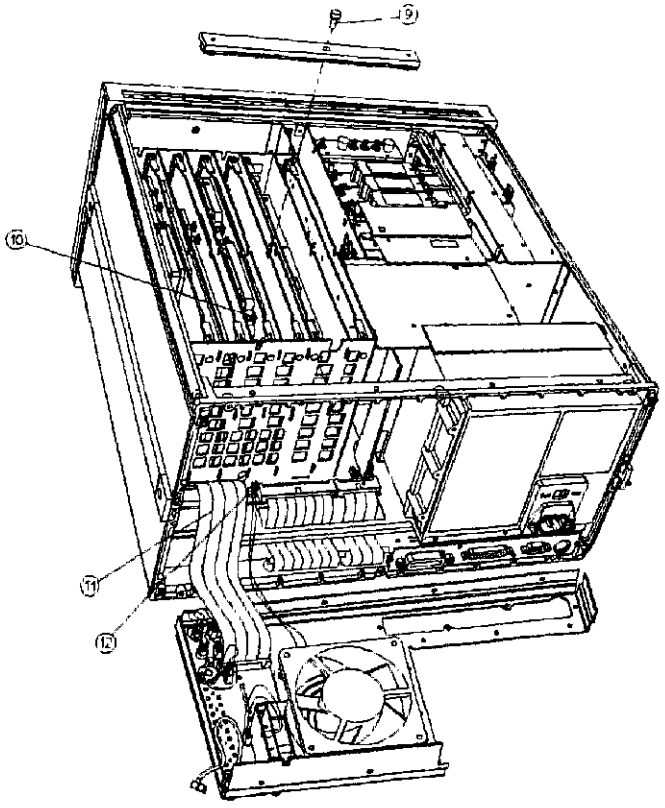
10. Pull the rear panel away from the frame. Disconnect the ribbon cable (item 11) from the motherboard connector pressing down and out. on the connector locks. Disconnect the wiring harness (item 12) from the motherboard.

Replacement

1. Reverse the order of the removal procedure.



Rear Panel Assembly



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Rear Panel Interface Board Assembly (A16)

Tools Required

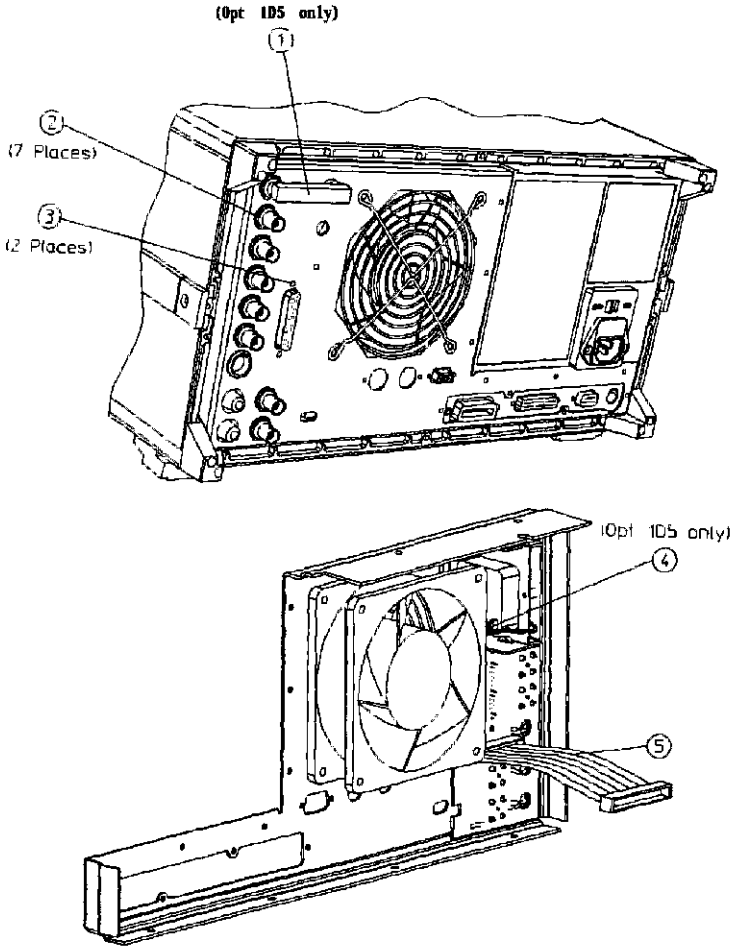
- 9/16 hex nut driver
- 3/16 hex nut driver
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD [electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top and bottom covers (refer to "Covers" in this chapter)
2. If the analyzer has option 1D5, remove the high-stability frequency reference jumper (item 1).
3. Remove the hardware that attaches the seven BNC connectors to the rear panel (item 2).
4. Remove the hardware that attaches the interface connector to the rear panel (item 3).
5. Remove the rear panel from the analyzer (refer to "Rear Panel Assembly" in this chapter).
6. If the analyzer has option 1D5, disconnect the cable (item 4) from the rear panel interface board
7. Disconnect the ribbon cable (item 5) from the rear panel interface board.

Replacement

1. Reverse the order of the removal procedure.


(Opt 1D5 only)
1
2
(7 Places)
3
(2 Places)
(Opt 1D5 only)
4
5
sg68ue

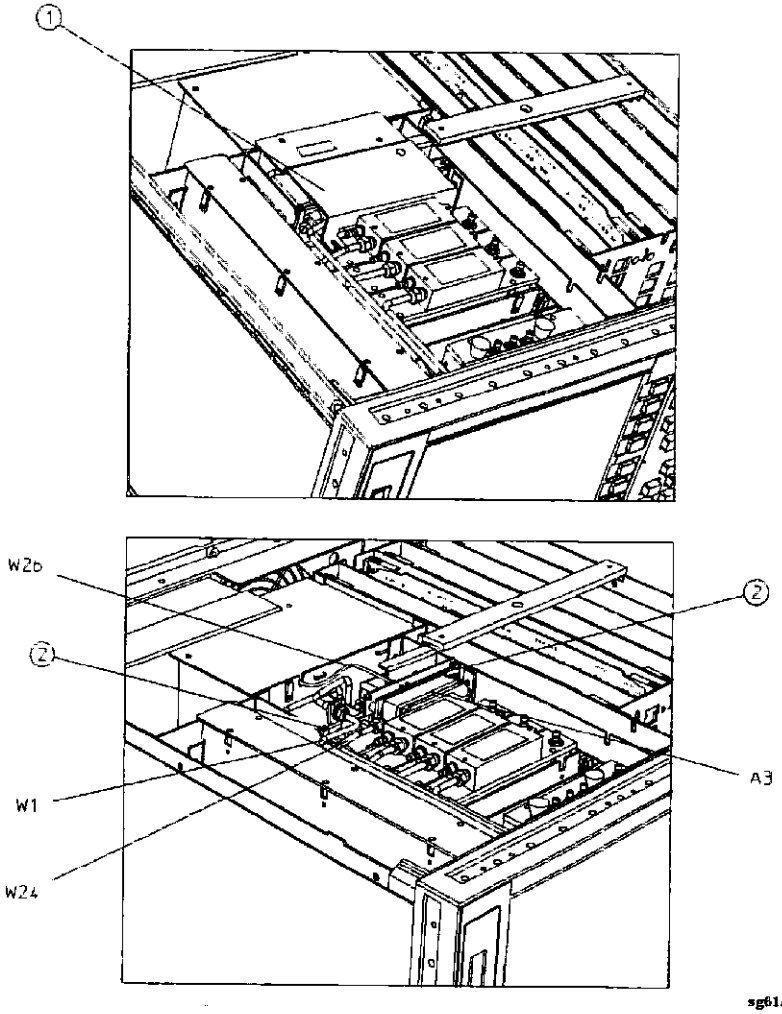
A3 Source Assembly

Tools Required

- T-15 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

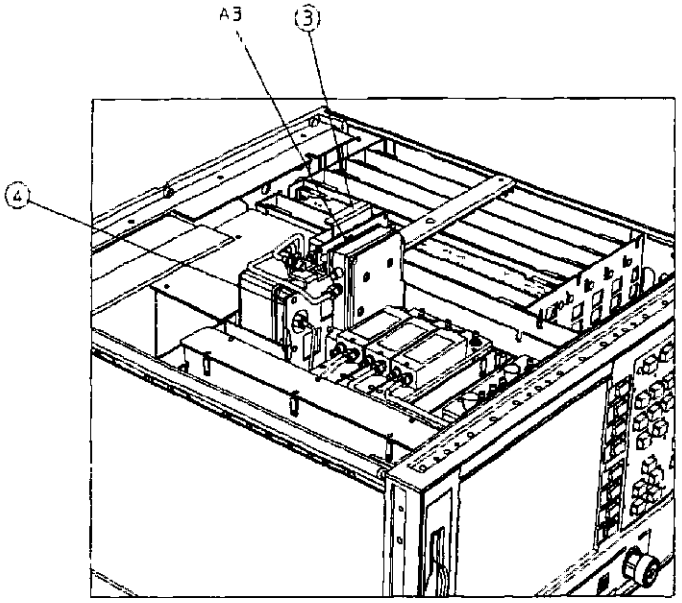
Removal

1. Disconnect the power cord and remove the top cover (refer to "Covers" in this chapter).
2. Remove the source bracket (item 1) by removing four screws. (It might be necessary to disconnect a flexible cable from the B sampler.)
3. Disconnect the flexible cable W26.
4. Disconnect the semirigid cable W1.
5. Lift the two retention clips (item 2) at the front and rear of the source assembly to an upright position.
6. Move W1 to the side while lifting the source high enough to provide wrench clearance for W24. To lift the A3 source assembly, use the source bracket handle (item 3).
7. Disconnect the semirigid cable W24.
8. Remove the source assembly from the instrument.



sg6120e

A3 Source Assembly



sg687e

Replacement

1. Check the connector pins on the motherboard before reinstallation.
2. Slide the edges of the sheet metal partition (item 4) into the guides at the sides of the source compartment. Press down on the module to ensure that it is well seated in the motherboard connector.
3. Push down the retention clips. Reconnect the two semirigid cables (W1 and W24) and one flexible cable (W26) to the source assembly.

Note When reconnecting semirigid cables, it is recommended that the connections be torqued to 10 in-lb.

4. Reinstall the source bracket.
5. Reconnect the flexible cable to the B sampler.

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A4, A5, A6 Samplers and A7 Pulse Generator

Tools Required

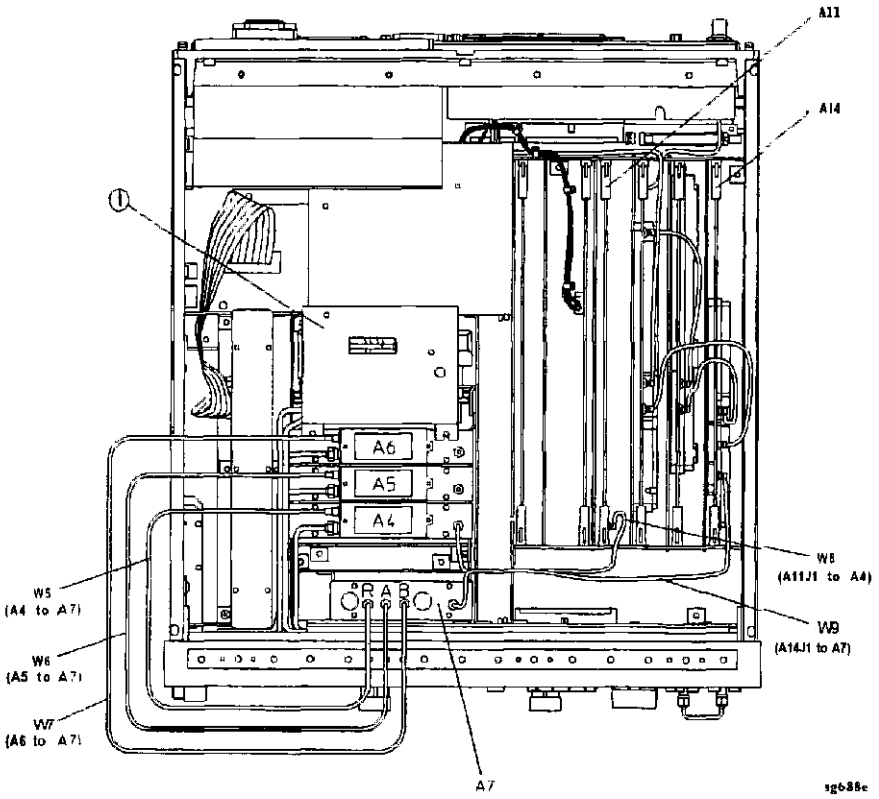
- T-10 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top cover (refer to "Covers" in this chapter).
2. To remove the B sampler (A6), you must remove the source bracket (item 1).
3. Disconnect all cables from the top of the sampler (A4/A5/A6) or pulse generator (A7).
4. Remove the screws from the top of each sampler assembly. Extract the assembly from the slot.

Note To remove the A (A5) or R (A4) sampler, first remove the cable on the B (A6) sampler.

Note If you are removing the pulse generator (A7), the grounding clip, which rests on top of the assembly, will become loose once the four screws are removed. Be sure to replace the grounding clip when reinstalling the pulse generator assembly.


A11
A14
1
A6
A5
A4
R A B
W5
(A4 to A7)
W6
(A5 to A7)
W7
(A6 to A7)
W8
(A11J1 to A4)
W9
(A14J1 to A7)
A7
sg688e

Replacement

1. Check the connector pins on the motherboard before reinstallation.
2. Reverse the order of the removal procedure.

Note

- When reconnecting semirigid cables, it is recommended that the connections be torqued to 10 in-lb.
- Be sure to route W8 and W9 as shown. No excess wire should be hanging in the A11 and A14 board slots. Routing the wires in this manner will reduce noise and crosstalk.

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A8, A10, A11, A12, A13, A14 Card Cage Boards

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

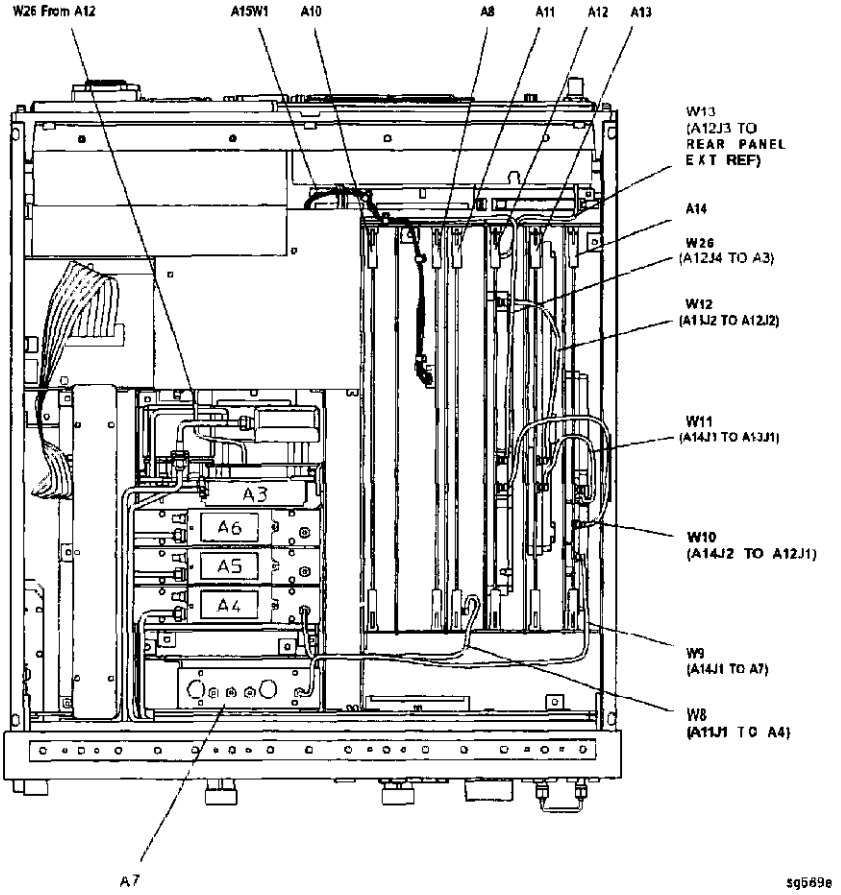
1. Disconnect the power cord and remove the top cover (refer to "Covers" in this chapter).
2. Remove the screw from the pc board stabilizer and remove the stabilizer.
3. Lift the two extractors located at each end of the board. Lift the board from the card cage slot, just enough to disconnect any flexible cables that may be connected to it.
4. Remove the board from the card cage slot.

Replacement

1. Check the connector pins on the motherboard before reinstallation.
2. Reverse the order of the removal procedure.

Note Be sure to route W8 and W9 as shown. No excess wire should be hanging in the A11 and A14 board slots. Routing the wires in this manner will reduce noise and crosstalk in the instrument.

A8, A10, A11, A12, A13, A14 Card Cage Boards



A9 CPU Board

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

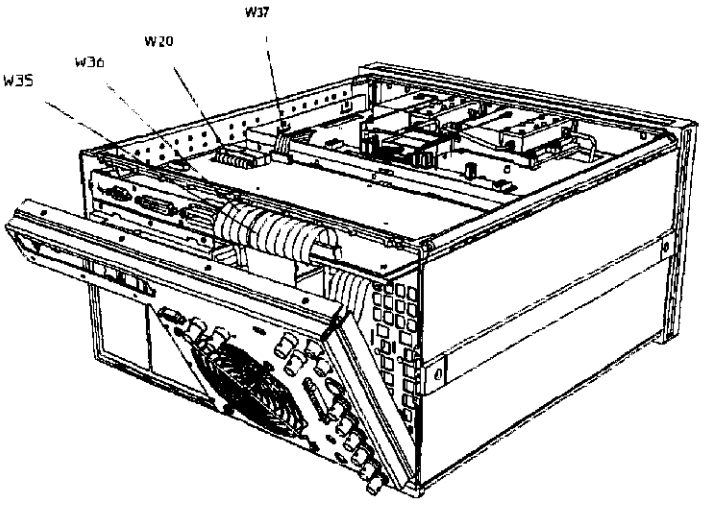
Removal

1. Disconnect the power cord.
2. Remove the top and bottom covers (refer to "Covers" in this chapter).
3. Remove the rear panel assembly, following steps 4 through 6 of "Rear Panel Assembly."
4. Turn the analyzer upside down.
5. Pull the rear panel away from the frame as shown in the following figure.
6. Disconnect the four ribbon cables (W20, W35, W36, and W37) from the CPU board (A9).
7. Remove the three screws (item 2) that secure the CPU board (A9) to the deck. Slide the board towards the front of the instrument so that it disconnects from the three standoffs (item 3).
8. Lift the board off of the standoffs.

Replacement

1. Reverse the order of the removal procedure.
2. Leave the bottom cover off in order to perform the post repair procedures located at the end of this chapter.

A9 CPU Board



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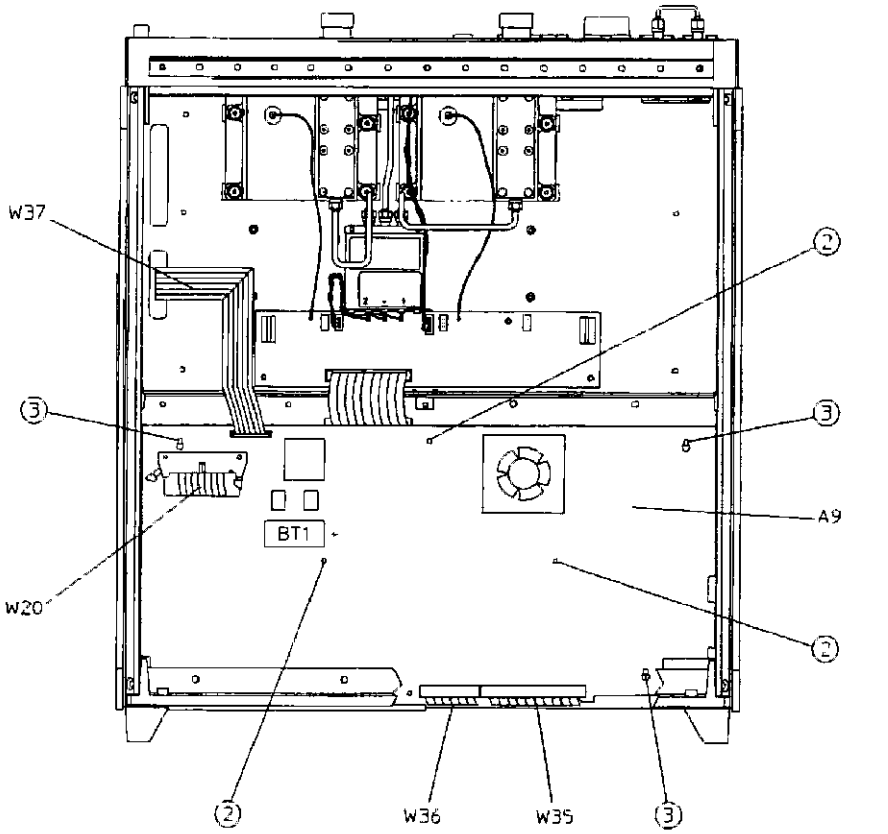
A9 CPU Board



sg690e

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A9BT1 Battery

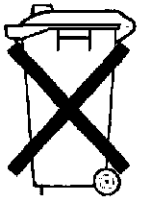
Tools Required

- T-10 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- soldering iron with associated soldering tools

Removal

1. Remove the A9 CPU/PIG board (refer to "A9 CPU Board" in this chapter).
2. Unsolder and remove A9BT1 from the A9 CPU/PIG board.

Warning **Battery A9BT1 contains lithium. Do not incinerate or puncture this battery. Dispose of the discharged battery in a safe manner.**



DO NOT THROW BATTERIES AWAY BUT
COLLECT AS SMALL CHEMICAL WASTE.

sk780a

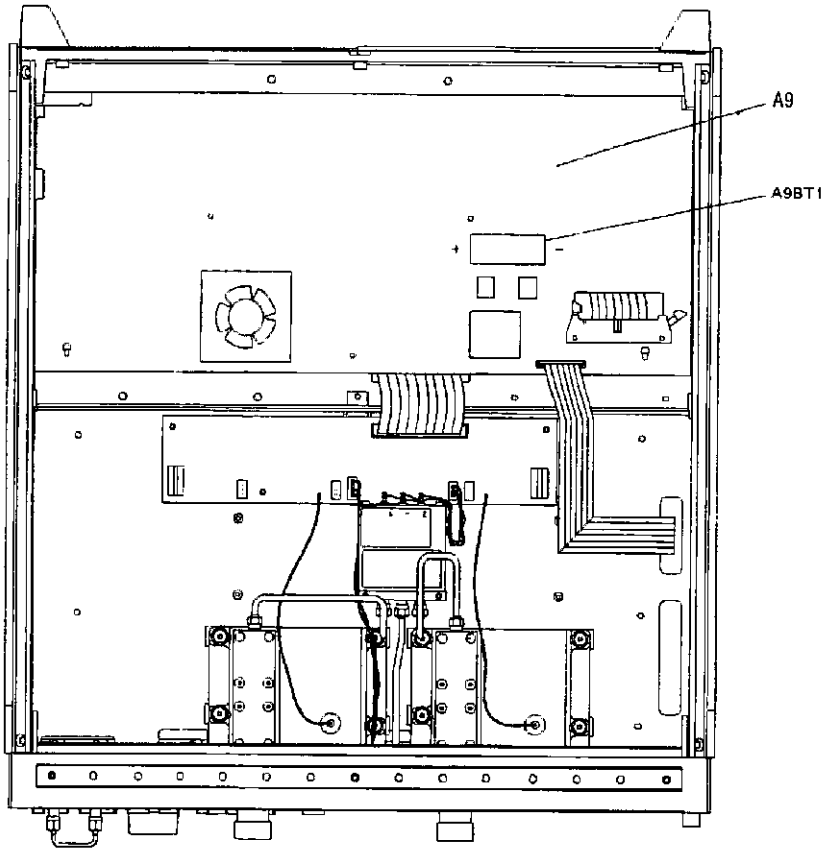
Replacement

1. Make sure the new battery is inserted into the A9 board with the correct polarity.

Warning **Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended.**

2. Solder the battery into place.
3. Replace the A9 CPU/PIG board (refer to "A9 CPU Board" in this chapter).

A9BT1 Battery



sg691e

A15 Preregulator

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter).
2. Remove the two remaining screws from the top of the rear frame.
3. Disconnect the wire bundle (A15W1) from A8J2 and A17J3.
4. Remove the preregulator (A15) from the frame.

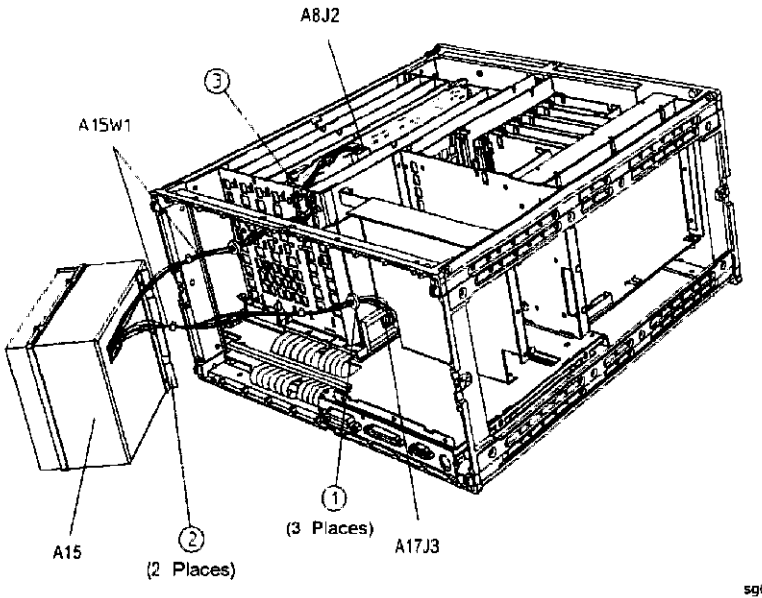
Replacement

1. Reverse the order of the removal procedure.

Note

- When reinstalling the preregulator (A15), make sure the three grommets (item 1) on A15W1 are seated in the two slots (item 2) on the back side of the preregulator and the slot (item 3) in the card cage wall.
- After reinstalling the preregulator (A15), be sure to set the line voltage selector to the appropriate setting, 115 V or 230 V.

A15 Preregulator



A17 Motherboard Assembly

Tools Required

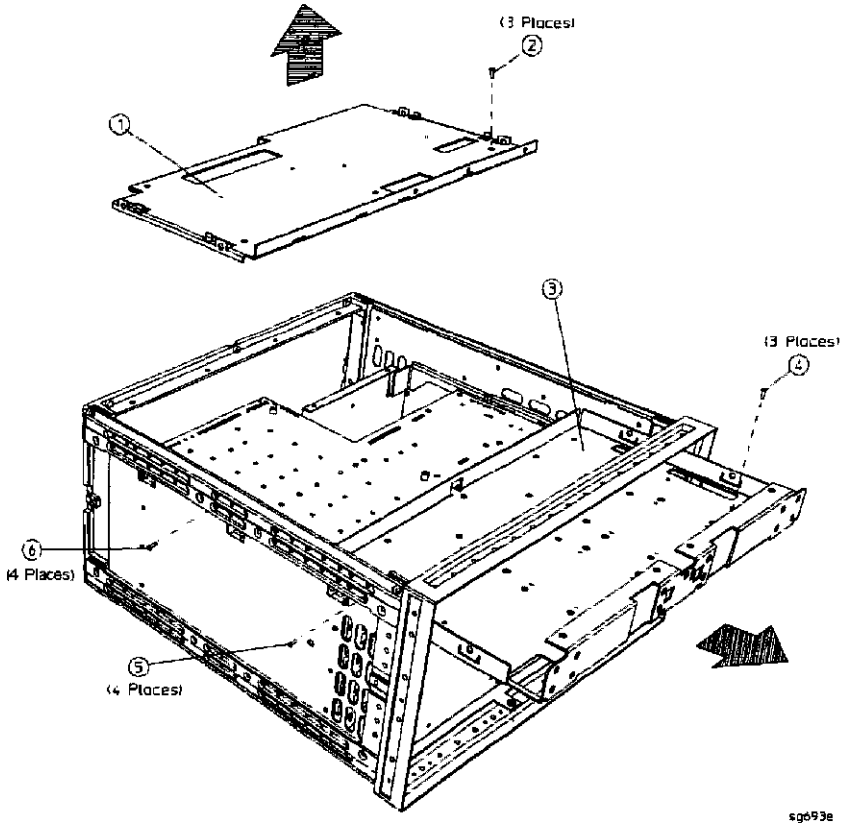
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- T-20 TORX screwdriver
- small slot screwdriver
- 2.5-mm hex-key driver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

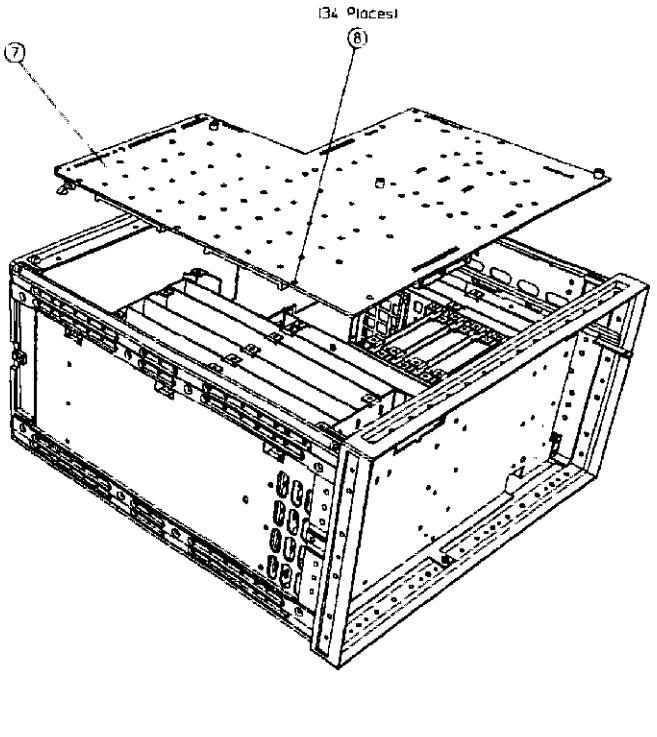
To remove the A17 motherboard assembly only, perform the following steps to remove all assemblies and cables that connect to the motherboard.

1. Disconnect the power cord and remove the top, bottom, and side covers (refer to "Covers" in this chapter).
2. Remove the front panel assembly (refer to "Front Panel Assembly" in this chapter).
3. Remove the rear panel assembly (refer to "Rear Panel Assembly" in this chapter).
4. Remove the preregulator (refer to "A15 Preregulator" in this chapter).
5. Remove the graphics processor (refer to "A19 Graphics Processor" in this chapter).
6. Remove the test set deck (item 3) by removing the three screws (item 4) from the bottom and four screws (item 5) from the side frames. For clarity, the figure on the next page does not show the assemblies attached to the test set deck.
7. Remove the CPU board (refer to "A9 CPU Board" in this chapter).
8. Remove the memory deck (item 1) by removing three screws (item 2) from the bottom and four screws (item 6) from the side frames.

9. Remove the source assembly (refer to "A3 Source Assembly" in this chapter).
10. Remove the samplers and pulse generator (refer to "A4, A5, A6 Samplers and A7 Pulse Generator" in this chapter).
11. Remove the card cage boards (refer to "A8, A10, A11, A12, A13, A14 Card Cage Boards" in this chapter). Continue with step 12 to remove the motherboard, or step 13 to remove the motherboard/card cage assembly.
12. To disconnect the motherboard (item 7), remove the 34 riv screws (item 8). ***Important: Do not misplace any of these screws.***



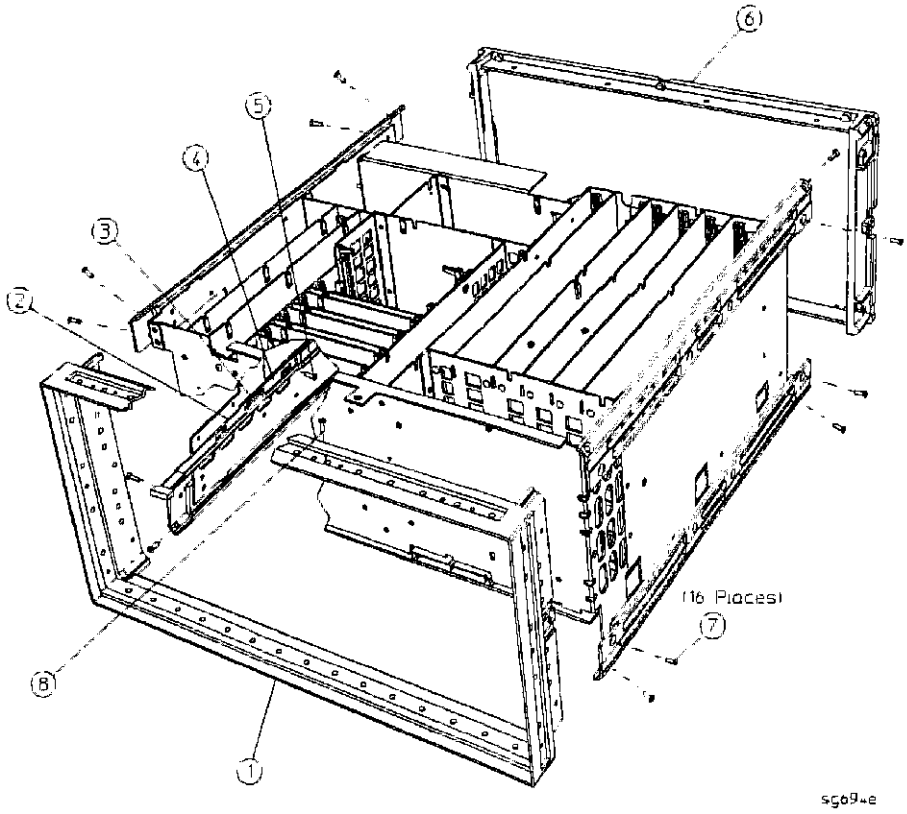
A17 Motherboard Assembly



sg610-3e

To remove the A17 motherboard assembly along with the card cage, continue with the following step:

13. Referring to the figure on the following page, remove the front frame (item 1) and rear frame (item 6) by removing the attaching screws (item 7). At this point, only the motherboard/card cage assembly should remain. This whole assembly is replaceable.



Replacement

1. Reverse the order of the removal procedure.

A19 Graphics Processor

Tools Required

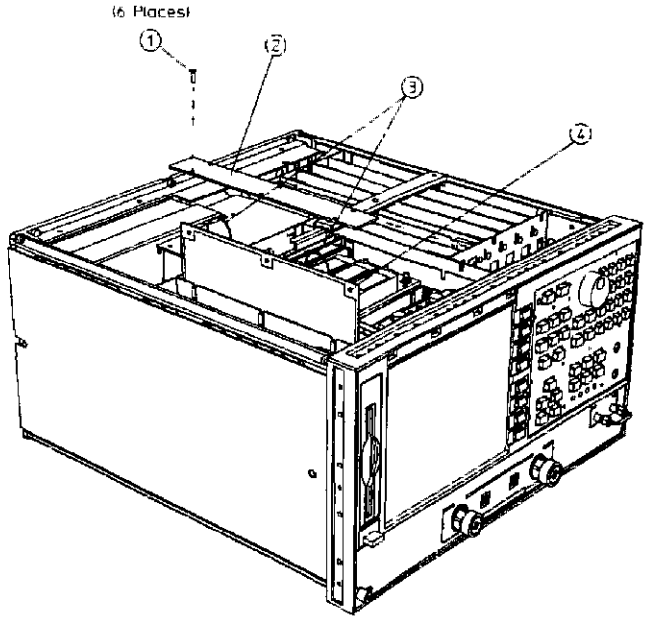
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord.
2. Remove the top cover (refer to "Covers" in this chapter) and front panel (refer to "Front Panel Assembly" in this chapter.)
3. Remove the six screws (item 1) from the GSP cover (item 2) and lift off.
4. Swing out the handles (item 3) and pull the GSP board (item 4) out of the analyzer.

Replacement

1. Check the connector pins on the motherboard before reinstallation.
2. Reverse the order of the removal procedure.



sg695e

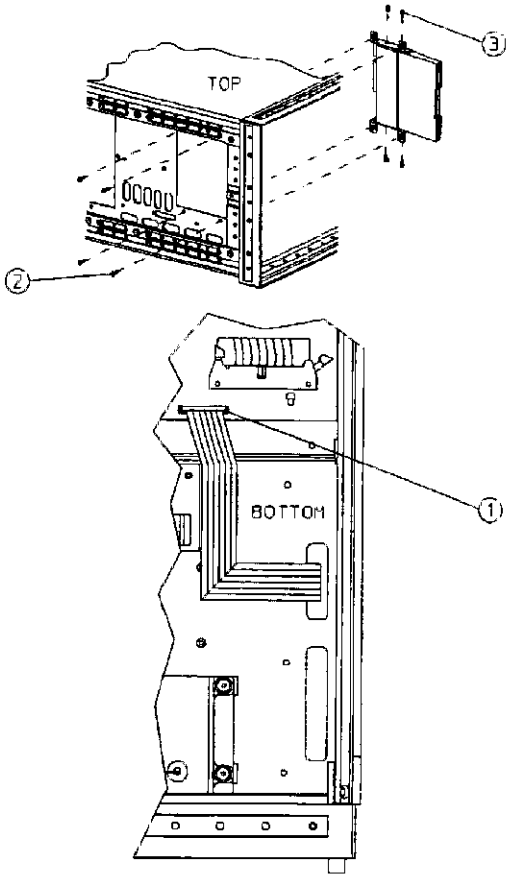
A20 Disk Drive Assembly

Tools Required

- 2-mm extended bit allen wrench
- T-8 TORX screwdriver
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- T-25 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top, bottom, and left side covers (refer to "Covers" in this chapter).
2. Remove the front panel (refer to "Front Panel Assembly" in this chapter).
3. Turn the instrument upside-down and disconnect the ribbon cable (item 1) from the CPU board.
4. Remove the four screws (item 2) that secure the disk drive bracket to the side of the frame.
5. Slide the disk drive out of the instrument.
6. Remove the four screws (item 3) that secure the disk drive to the bracket.


TOP
BOTTOM
1
2
3
sg696a

A20 Disk Drive Assembly

Replacement

1. While the disk drive is horizontal and on a flat surface, attach the disk drive bracket with four screws.
2. Slide the disk drive into the instrument.
3. Loosely secure the disk drive bracket to the side of the frame with four screws.
4. Turn the instrument upside-down and connect the ribbon cable to the CPU board.
5. Replace the front panel with the exception of fastening the top left screw (refer to "Front Panel Assembly" in this chapter).
6. While adjusting the position of the disk drive, tighten the screws that secure the disk drive bracket to the side of the frame.
7. Insert a disk into the disk drive and then eject the disk.

   - If the disk drive door operation is satisfactory, continue with step 9.

   - If the disk drive door operation is not satisfactory, continue with step 8.
8. Loosen and then retighten the four screws that secure the disk drive to the disk drive bracket:

   a. Loosen the three screws that are readily accessible.

   b. Loosen the uppermost, frontmost screw through the top left access hole in the front frame.

   c. After disk drive tension has been released, retighten all four screws.
9. Finish the front panel replacement procedure by fastening the remaining screw (top left) to the front panel.
10. Replace the covers (refer to "Covers" in this chapter)

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A21, A22 Test Port Couplers

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD [electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

1. Disconnect the power cord and remove the bottom cover (refer to "Covers" in this chapter).
2. Disconnect the small bias wire from the test set interface board (A25).

   For coupler A21 disconnect the gray wire (A21W1).
   For coupler A22 disconnect the gray wire (A22W1).
3. Disconnect the two semirigid cables from the coupler assembly.

   For coupler A21 disconnect W3 and W31.
   For coupler A22 disconnect W4 and W32.
4. Remove the four screws, washers, and pressure springs that secure the coupler to the test set deck. Remove the coupler.
5. Remove the pressure springs.

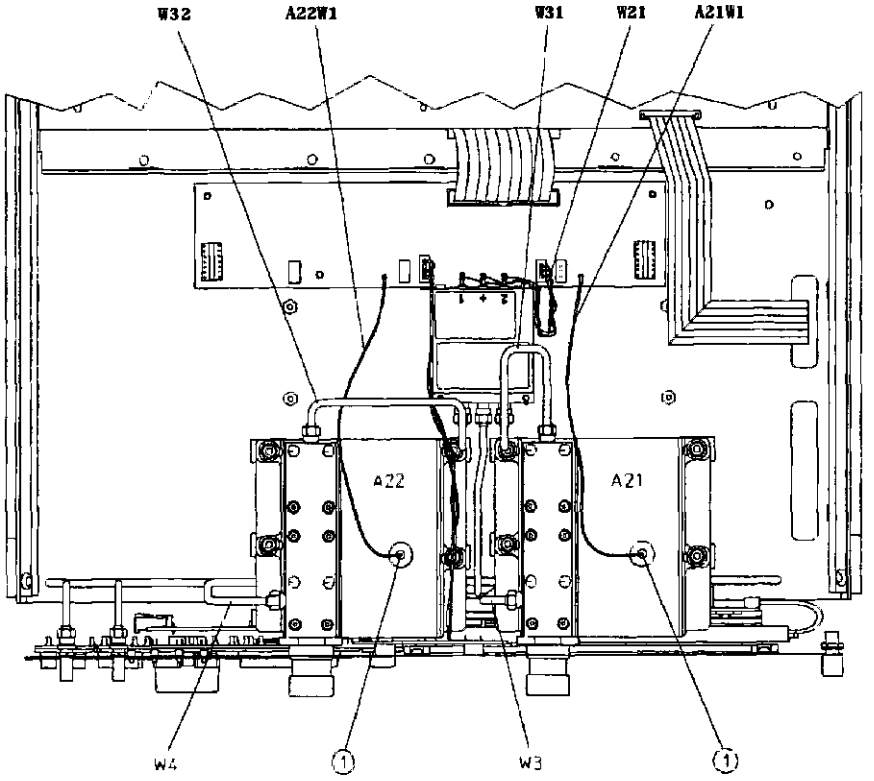
Replacement

1. Reverse the order of the removal procedure.

Note - If you're installing a new coupler, the gold lead on the feedthru capacitor (item 1) must be carefully bent at 90 degrees to prevent it from shorting to the bottom cover.

When reconnecting semirigid cables, it is recommended that the connections be torqued to 10 in-lb.

A21, A22 Test Port Couplers



sg697e

A23 LED Board

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

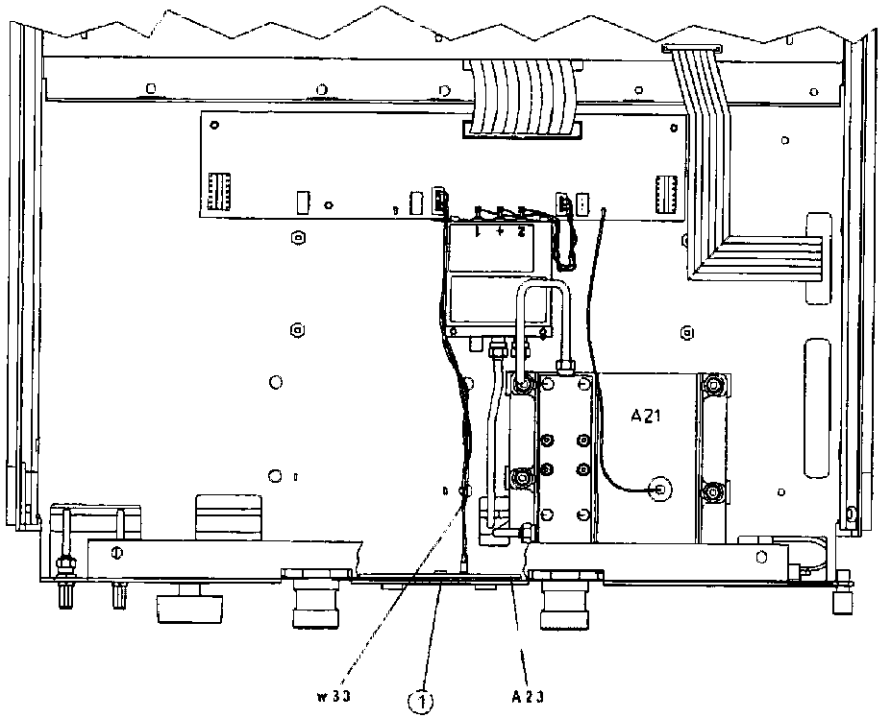
Removal

1. Disconnect the power cord and remove the bottom cover (refer to "Covers" in this chapter).
2. Remove the front panel (refer to "Front Panel Assembly" in this chapter).
3. Remove the A22 test port coupler (refer to "A21, A22 Test Port Couplers" in this chapter).
4. Disconnect W33 from the LED board (A23).
5. Remove the screw (item 1) from the front of the test set deck.
6. Remove the LED board (A23).

Replacement

1. Reverse the order of the removal procedure.

A23 LED Board



sg698e

A24 Transfer Switch

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

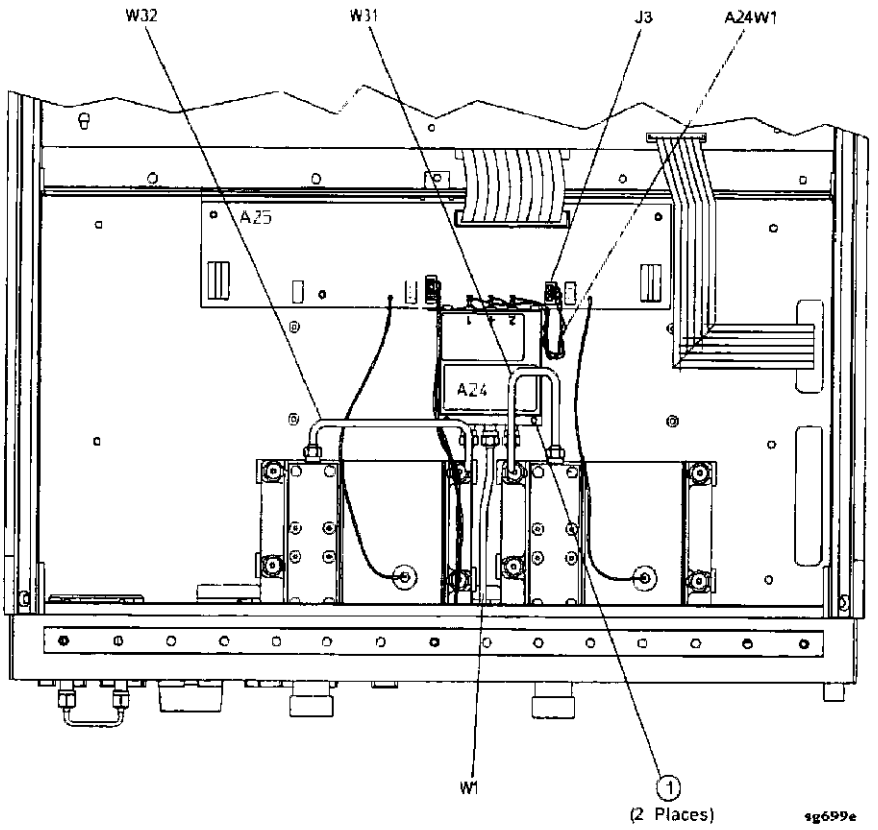
1. Disconnect the power cord and remove the bottom cover (refer to "Covers" in this chapter).
2. Disconnect A24W1 from J3 on the test set interface board (A25).
3. Disconnect the three semirigid cables (W1, W31, and W32) from the transfer switch (A24).
4. Remove the two screws (item 1) that secure the transfer switch.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semirigid cables, it is recommended that the connections be torqued to 10 in-lb.

A24 Transfer Switch



A25 Test Set Interface

Tools Required

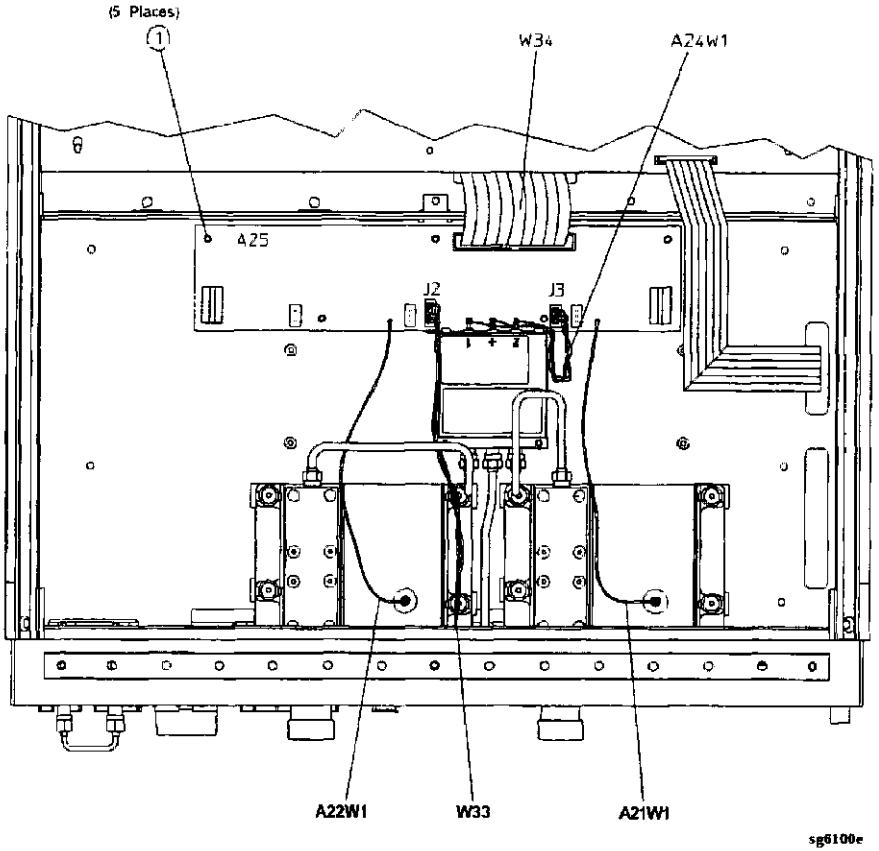
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the bottom cover (refer to "Covers" in this chapter).
2. Disconnect all cables and wires (A21 W1, A22W1, W33, and W34) from the test set interface board (A25).
3. Remove the five screws (item 1) that secure the test set interface board.

Replacement

1. Reverse the order of the removal procedure.


(5 Places)
1
W34
A24W1
A25
J2
J3
A22W1
W33
A21W1
sg6100e

A26 High Stability Frequency Reference (Option 1D5) Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- 9/16-inch hex-nut driver
- ESD (electrostatic discharge) grounding wrist strap

Removal

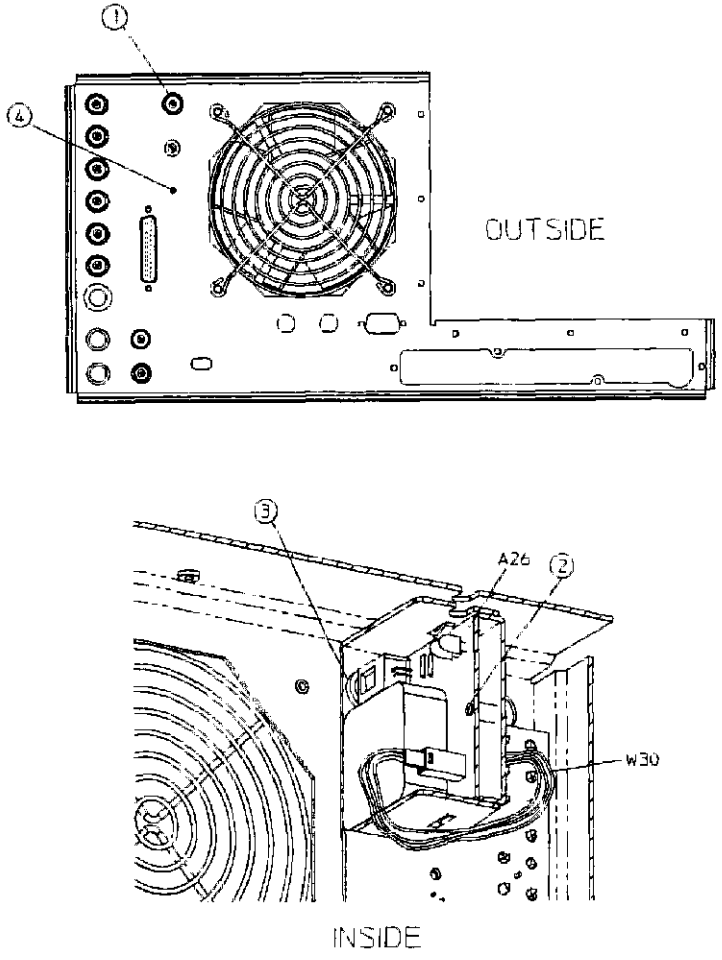
1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter).
2. Disconnect W30 from the high stability frequency reference board (A26).
3. Remove the BNC connector nut and washer from the "10 MHz PRECISION REFERENCE" connector (item 1) on the rear panel.
4. Remove the screw (item 4) that attaches the 1D5 assembly to the rear panel.
5. Remove the screw (item 2) that secures the high stability frequency reference board (A26) to the bracket.
6. Slide the board out of the bracket. Be careful not to lose the plastic spacer washer (item 3) that is on the BNC connector as the board is being removed.

Replacement

1. Reverse the order of the removal procedure.

Note Before reinserting the high stability frequency reference board (A26) into the bracket, be sure the plastic spacer washer (item 3) is on the BNC connector.

A26 High Stability Frequency Reference (Option 1D5) Assembly



sg6101e

B1 Fan Assembly

Tools Required

- 2.5mm hex-key driver
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

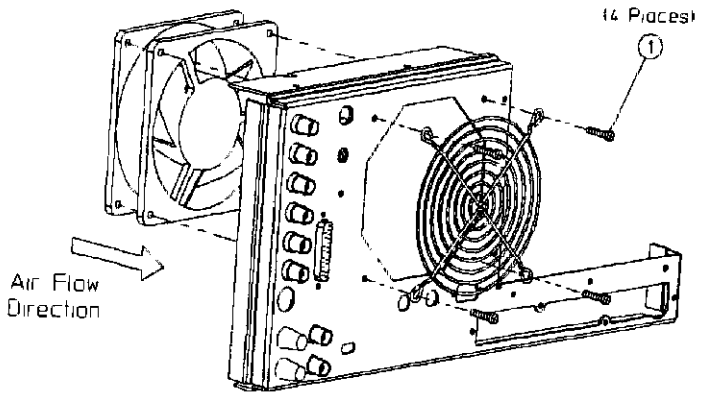
1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter).
2. Remove the four screws (item 1) that secure the fan and fan cover to the rear panel.

Replacement

1. Reverse the order of the removal procedure.

Note The fan should be installed so that the direction of the air flow is away from the instrument. There is an arrow on the fan chassis indicating the air flow direction.

B1 Fan Assembly



sg659e

Post-Repair Procedures for HP 8753E

The following table lists the additional service procedures which you must perform to ensure that the instrument is working correctly, following the replacement of an assembly. These procedures can be located in either Chapter 2 or Chapter 3.

Perform the procedures in the order that they are listed in the table.

Table 14-1. Related Service Procedures

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A1 Front Panel Keyboard	None	Service Test 0 Service Test 23
A2 Front Panel Interface	None	Service Test 0 Service Test 23 Service Test 12 Tests 66 - 80
A3 Source	A9 Switch Positions Source Def CC (Test 44) Pretune Default CC (Test 45) Analog Bus CC (Test 46) Source Pretune CC (Test 48) RF Output Power CC (Test 47) Sampler Magnitude and Phase CC (Test 53) Cavity Oscillator Frequency CC (Test 54) Source Spur Avoidance Tracking EEPROM Backup Disk	Test Port Output Frequency Range and Accuracy Test Port Output Power Accuracy Test Port Output Power Range and Linearity Test Port Output/Input Harmonics (Option 002 only) or System Verification
A4/A5/A6 Samplers	A9 Switch Positions Sampler Magnitude and Phase CC (Test 53) IF Amplifier CC (Test 51) EEPROM Backup Disk	Minimum R Channel Level (if R sampler replaced) Test Port Crosstalk Test Port Input Frequency Response or System Verification
A7 Pulse Generator	A9 Switch Positions Sampler Magnitude and Phase CC (Test 53) EEPROM Backup Disk	Test Port Input Frequency Response Test Port Frequency Range and Accuracy or System Verification
A8 Post Regulator	A9Switch Positions Cavity Oscillator Frequency CC (Test 54) Source Spur Avoidance Tracking EEPROM Backup Disk	Service Test 0 Check A8test paint voltages

Table 14-1. Related Service Procedures (2 of 3)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A9 CPU (EEPROM Backup Disk Available)	A9 Switch Positions Load Firmware CC Retrieval Serial Number CC (Test 55) Option Number CC (Test 56)	Operator's Check Service Test 21 Service Test 22
A9 CPU (EEPROM Backup Disk Not Available)	A9 Switch Positions Load Firmware Serial Number CC (Test 55) Option Number CC (Test 56) Source Def CC (Test 44) Pretune Default CC (Test 45) Analog Bus CC (Test 46) Cal Kit Default (Test 57) Source Pretune CC (Test 48) RF Output Power CC (Test 47) Sampler Magnitude and Phase CC (Test 53) ADC Linearity CC (Test 52) IF Amplifier CC (Test 51) Cavity Oscillator Frequency CC (Test 54) EEPROM Backup Disk	Test Port Output Frequency Range and Accuracy Test Port Output Power Accuracy Test Port Output Power Range and Linearity Test Port Receiver Dynamic Accuracy Test Port Input Frequency Response or System Verification
A10 Digital IF	A9 Switch Positions Analog Bus CC (Test 46) Sampler Magnitude and Phase CC (Test 53) ADC Linearity CC (Test 52) IF Amplifier CC (Test 51) EEPROM Backup Disk	Test Port Input Noise Floor Level Test Port Crosstalk System Trace Noise or System Verification
A11 Phase Lock	A9 Switch Positions Analog Bus CC (Test 46) Pretune Default CC (Test 45) Source Pretune CC (Test 48) EEPROM Backup Disk	Minimum R Channel Level TestPort Output FrequencyRange and Accuracy or System Verification

Table 14-1. Related Service Procedures (3 of 3)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A12 Reference	A9 Switch Positions High/Low Band Transition Frequency Accuracy EEPROM Backup Disk	Test Port Output Frequency Range and Accuracy
A13 Fractional-N (Analog)	A9 Switch Positions Fractional-N Spur and FM Sideband EEPROM Backup Disk	Test Port Output Frequency Range and Accuracy
A14 Fractional-N (Digital)	A9 Switch Positions Fractional-N Frequency Range Fractional-N Spur Avoidance and FM Sideband EEPROM Backup Disk	Test Port Output Frequency Range and Accuracy or System Verification
A15 Preregulator	None	Self-Test
A16 Rear Panel Interface	None	Internal Test 13, Rear Panel
A17 Motherboard	None	Observation of Display Tests 66 - 80
A18 Display	None	Observation of Display Tests 66 - 80
A19 Graphics System Processor	None	Observation of Display Tests 59 - 80

11

Error Terms

The analyzer generates and stores factors in internal arrays when a measurement error-correction (measurement calibration) is performed. These factors are known by the following terms:

- error terms
- E-terms
- measurement calibration coefficients

The analyzer creates error terms by measuring well-defined calibration devices over the frequency range of interest and comparing the measured data with the ideal model for the devices. The differences represent systematic (repeatable) errors of the analyzer system. The resulting calibration coefficients are good representations of the systematic error sources. for details on the various levels of error-correction, refer to the "Optimizing Measurement Results" chapter of the *HP 8719D/20D/22D Network Analyzer User's Guide.* For details on the theory of error-correction, refer to the "Application and Operation Concepts" chapter of the *HP 8719D/20D/22D Network Analyzer User's Guide.*

Error Terms Can Also Serve a Diagnostic Purpose

Specific parts of the analyzer and its accessories directly contribute to the magnitude and shape of the error terms. Since we know this correlation and we know what typical error terms look like, we can examine error terms to monitor system performance (preventive maintenance) or to identify faulty components in the system (troubleshooting).

- **Preventive Maintenance:** A stable, repeatable system should generate repeatable error terms over long time intervals, for example, six months. If you make a hardcopy record (print or plot) of the error terms, you can periodically compare current error terms with the record. A sudden shift in error terms reflects a sudden shift in systematic errors, and may indicate the need for further troubleshooting. A long-term trend often reflects drift.

connector and cable wear, or gradual degradation, indicating the need for further investigation and preventive maintenance. Yet, the system may still conform to specifications. The cure is often as simple as cleaning and gaging connectors or inspecting cables.

- **Troubleshooting:** If a subtle failure or mild performance problem is suspected, the magnitude of the error terms should be compared against values generated previously with the same instrument and calibration kit. This comparison will produce the most precise view of the problem.

  However, if previously generated values are not available, compare the current values to the typical values listed in Table 11-2, and shown graphically on the plots in this chapter. If the magnitude exceeds its limit, inspect the corresponding system component. If the condition causes system verification to fail, replace the component.

  Consider the following while troubleshooting:

  - All parts of the system, including cables and calibration devices, can contribute to systematic errors and impact the error terms
  - Connectors must be clean, gaged, and within specification for error term analysis to be meaningful.
  - Avoid unnecessary bending and flexing of the cables following measurement calibration, minimizing cable instability errors.
  - Use good connection techniques during the measurement calibration. The connector interface must be repeatable. Refer to the "Principles of Microwave Connector Care" section in the "Service Equipment and Analyzer Options" chapter for information on connection techniques and on cleaning and gaging connectors.
  - Use error term analysis to troubleshoot minor, subtle performance problems. Refer to the "Start Troubleshooting Here" chapter if a blatant failure or gross measurement error is evident.
  - It is often worthwhile to perform the procedure twice (using two distinct measurement calibrations) to establish the degree of repeatability. If the results do not seem repeatable, check all connectors and cables.

Measurement Calibration Procedure

1. Refer to the "Measurement Calibration" section in Chapter 2, "System Verification and Performance Tests." and perform the full 2-port calibration with the following modifications:
2. For the reflection measurements (short, open, loads), connect the calibration device directly to the test port instead of to a reference test port. Use the female devices for port, 1. Adapt the male devices for port 2.
3. For the reflection measurements, use a cable configuration (a single cable or cable pair) that is consistent with the normal use of the system.
4. For the isolation measurement, select from the following two options:
   - If you will be measuring devices with a dynamic range less than 90 dB, press:

     [OMIT ISOLATION] [ISOLATION DONE]

   - If you will be measuring devices with a dynamic range greater than 90 dB, follow these steps:

     a. Leave the cables connected and connect impedance-matched loads to the test ports (or reference test ports).

Note If you will be measuring highly reflective devices, such as filters, use the test device, connected to the reference plane and terminated with a load, for the isolation standard.

b. Press **[Avg]** [AVERAGING on] [AVERAGING FACTOR] **[16] [x1]** to change the averaging to at least 16.

c. Press **[Avg]** [IF BW] **[10] [x1]** to change the IF bandwidth to 10 Hz.

d. Press **[Cal]** [RESUME CAL SEQUENCE] [ISOLATION] [DO BOTH FWD + REV].

e. Return the averaging to the original state of the measurement, and press **[Cal]** [RESUME CAL SEQUENCE DONE 2-PORT CAL].

The following table lists the calibration coefficients along with their corresponding test numbers. You may wish to refer to this table when performing the "Error Term Inspection" procedure.

Table 11-1. Calibration Coefficient Terms and Tests

Calibration Coefficient	Calibration Type				Test Number
	Response	Response and Isolation*	1-port	2-port†	
1	E_R or E_T	E_X (E_D)	E_D	E_{DF}	31
2		E_T (E_R)	E_S	E_{SF}	32
3			E_R	E_{RF}	33
4				E_{XF}	34
5				E_{LF}	35
6				E_{TF}	36
7				E_{DR}	37
8				E_{SR}	38
9				E_{RR}	39
10				E_{XR}	40
11				E_{LR}	41
12				E_{TR}	42

NOTES:

Meaning of first subscript: D=directivity; S=source match; R=reflection tracking; X=crosstalk; L=load match; T=transmission tracking

Meaning of second subscript: F=forward; R=reverse

* Response and Isolation cal yields: E_X or E_T if a transmission parameter (S_{21}, S_{12}) or E_D or E_R if a reflection parameter (S_{11}, S_{22})

† one-path, 2-port cal duplicates arrays 1 to 6 in arrays 7 to 12.

Error Term Inspection

Note If the correction is not active, press **[Cal]** [CORRECTION ON].

1. Press **[System]** [SERVICE MENU] [TESTS] **[31]** **[x1]** [EXECUTE TEST].

   The analyzer copies the first calibration measurement trace for the selected error term into memory and then displays it. Table 11-1 lists the test numbers.

2. Press **[Scale Ref]** and adjust the scale and reference to study the error term trace.

3. Press **[Marker Fctn]** and use the marker functions to determine the error term magnitude.

4. Compare the displayed measurement trace to the trace shown in the following "Error Term descriptions" section, and to previously measured data. If data is not available from previous measurements, refer to the typical uncorrected performance specifications listed in Table 11-2 and Table 11-3.

5. Make a hardcopy of the measurement results:

   a Connect a printing or plotting peripheral to the analyzer.

   b. Press **[Local]** [SYSTEM CONTROLLER] [SET ADDRESSES] and select the appropriate peripheral to verify that, the HP-IB address is set correctly on the analyzer.

   c. Press **[Save/Recall]** and then choose either [PRINT] or [PLOT].

   d. Press **[Display]** [MORE] [TITLE] and title each data trace so that you can identify it later.

Note For detailed information on creating hardcopies, refer to "Printing, Plotting, and Saving Measurement Results" in the *HP 8719D/20D/22D Network Analyzer User's Guide*

6. Repeat steps 1 through 5 for each test number that corresponds to a calibration coefficient (see Table 11-1).

If Error Terms Seem Worse than Typical Values

1. Perform a system verification to verify that the system still conforms to specifications.
2. If system verification fails, refer to "Start Troubleshooting Here."

Uncorrected Performance

The following tables show typical performance without error-correction. RF cables are not used except as noted. Related error terms should be within these values.

Table 11-2.
HP 8719D/8720D Characteristics Without Error-Correction

Parameter & Option	Frequency Range			
	0.05 to 0.6 GHz	0.6 to 2 GHz	2 to 8 GHz	8 to 20 GHz
Directivity[1]	27 dB	27 dB	21 dB	16 dB
Source Match (Standard)	12 dB	12 dB	10 dB	8 dB
Source Match (Option 400)	20 dB	20	12 dB	10 dB
Source Match (Option 007)	16 dB	20 dB	14 dB	11 dB
Source Match (Option 085)	18 dB	18 dB	14 dB	8 dB
Load Match (Standard)	22 dB	20 dB	12 dB	10 dB
Load Match (Option 400)	20 dB	17 dB	12 dB	10 dB
Load Match (Option 007)	26 dB	24 dB	15 dB	12 dB
Load Match (Option 085)	26 dB	24 dB	15 dB	10 dB
Reflection Tracking[2]	±3 dB	±3 dB	±3 dB	±3 dB
Transmission Tracking[2]	±3 dB	±3 dB	±3 dB	±3 dB
Crosstalk[2]	96 dB	95 dB	96 dB	90 dB

1 Includes effect of HP 85131D cable set on test ports.

2 Excludes 0/-5 dB slope, characteristic, in magnitude response from 0.84 to 40 GHz and rolloff below 0.84 Ghz, which is characteristically -3 dB at 500 MHz, -15 dB at 100 MHz, and -20 dB at 50 MHz

Table 11-3.
HP 8722D Characteristics Without Error-Correction

Parameter & Option	Frequency Range			
	0 05 to 2 GHz	2 to 8 GHz	8 to 20 GHz	20 to 40 GHz
Directivity	23 dB	21 dB	16 dB	16 dB
Source Match (Standard, Option 400)	17 dB	12 dB	11 dB	7 dB
Source Match (Option 007, Option 085)	20 dB	15 dB	11 dB	8 dB
Load Match[1] (Standard, Option 400)	18 dB	16 dB	12 dB	10 dB
Load Match (Option 007, Option 085)	21 dB	17 dB	13 dB	10 dB
Reflection Tracking[2]	±3 dB	±3 dB	±3 dB	±3 dB
Transmission Tracking[12]	±3 dB	±3 dB	±3 dB	±3 dB
Crosstalk	95 dB	95 dB	88 dB	85 dB

1 Measured with RF cables

2 Excludes 0/-5 dB slope, characteristic, in magnitude response from 0.84 to 40 GHz and rolloff below 0.84 GHz, which is characteristically -3 dB at 500 MHz, -15 dB at 100 MHz, and -20 dB at 50 MHz

Error Term Descriptions

The error term descriptions in this section include the following information:

- significance of each error term
- typical results following a full 2-port error-correction
- guidelines to interpret each error term

The same description applies to both the forward (F) and reverse (R) terms. The plots shown with each are typical of a working system following a full 2-port calibration as performed in "Measurement Calibration Procedure," above.

It may be helpful to define some of the terms used in the error term descriptions that. follow:

- **R signal path:** refers to the reference signal path. It includes the A58 M/A/D/S, A64 R sampler, and associated semi-rigid coax cables.
- **A input path:** refers to the port 1 input path and includes the A58 M/A/D/S, A69 step attenuator, S4 transfer switch, A61 bias tee, A62 directional coupler, A65 A sampler, and associated semi-rigid coax cables.
- **B input path:** refers to the port 2 input path and includes the A58 M/A/D/S, A69 step attenuator, S4 transfer switch, A60 bias tee, A63 directional coupler, A66 B sampler, and associated semi-rigid coax cables

Directivity (EDF and EDR)

These are the uncorrected forward and reverse directivity error terms of the system. The directivity error of the test port is determined by measuring the S11 and S22 reflection of the calibration kit load. The load has a much better return loss specification than does the uncorrected test port, therefore any power detected from this measurement is assumed to be due to directivity error.

Significant System Components. The load used in the calibration is the most important component. The test port connector, the cable, and the coupler also greatly affect the measured directivity error.

Affected Measurements. The measurements most affected by directivity errors are measurements of low reflection devices; highly reflective device measurements

will appear normal.

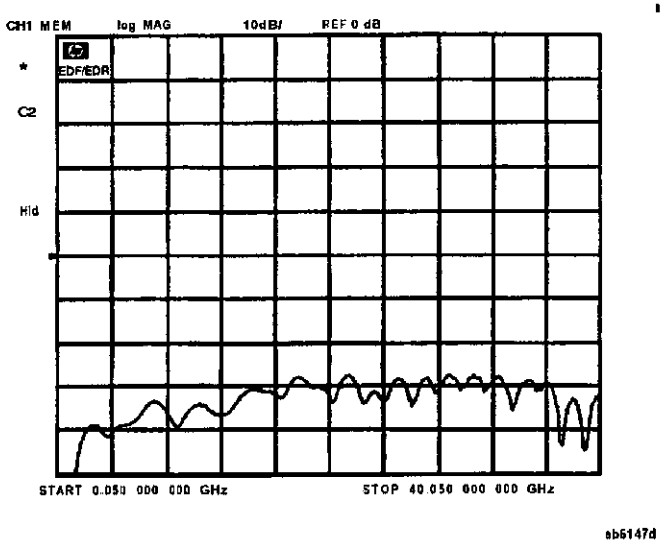


Figure 11-1. Typical EDF/EDR Without Cables

Source Match (ESF and ESR)

Description

These are the forward and reverse uncorrected source match terms of the driven port. They are obtained by measuring the reflection (S11, S22) of an open and then a short connected directly to the ports. Source match is a measure of the match between the coupler and test set connector, as well as the match between all components from the source to the output port.

Significant System Components. The open and short calibration devices are important, as are the coupler and test port connectors. The power splitter, bias tees, step attenuator, and transfer switch may also contribute to source match errors.

Affected Measurements. The measurements most affected by source match errors are reflection and transmission measurements of highly reflective DUTs.

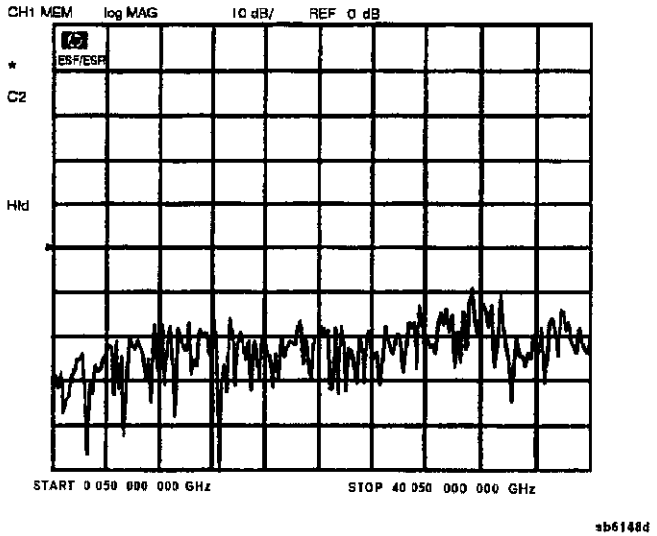


Figure 11-2. Typical ESF/ESR Without Cables

Reflection Tracking (ERF and ERR)

Reflection Tracking is the difference between the frequency response of the reference path (R path) and the frequency response of the reflection test path (A or B input path). These error terms are characterized by measuring the reflection (S11,S22) of the open and the short during the measurement calibration. Note that coupler response is included in this error term. Typically this appears as a slope of 0/-5 dB from 0.84 GHz to 40 GHz and a roll-off below 0.84 GHz, which is typically -3 dB at 500 MHz, -15 at 100 MHz, and -20 at 50 MHz.

Significant System Components. The open and short calibration devices have an effect on reflection tracking. But large variations in this error term may indicate a problem in one of the signal paths. Suspect the R signal path if the problem appears in both ERF and ERR. Troubleshoot the A or B input paths first if only one reflection tracking term is affected.

Affected Measurements. All reflection measurements (high or low return loss) are affected by the reflection tracking errors.

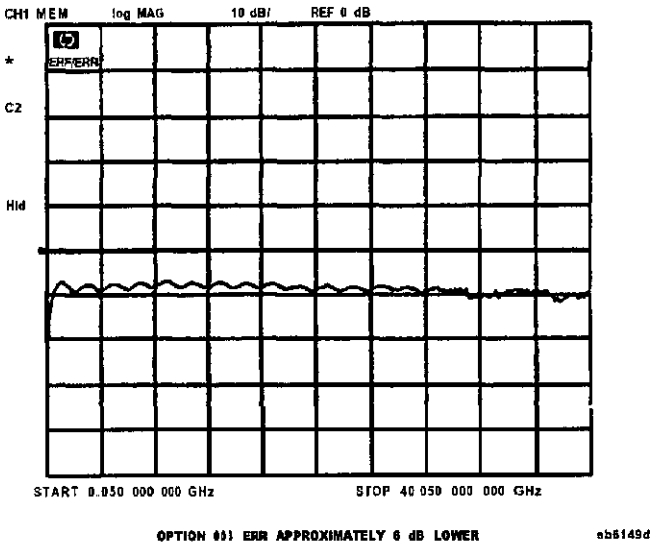


Figure 11-3. Typical ERF/ERR

Isolation (Crosstalk, EXF and EXR)

These are the uncorrected forward and reverse isolation error terms that represent leakage between the test ports and the signal paths. The isolation error terms are characterized by measuring transmission (S21, S12) with loads attached to both ports during the measurement calibration. Since these terms are low in magnitude, they are usually noisy (not very repeatable). The error term magnitude changes dramatically with IF bandwidth: a 10 Hz IF bandwidth must be used in order to lower the noise floor beyond the crosstalk specification. Using averaging will also reduce the peak-to-peak noise in this error term.

Significant System Components. Loose cable connections or leakage between components in the lower box are the most likely cause of isolation problems. The transfer switch, bias tees, couplers, and samplers are the most susceptible components.

Affected Measurements. Isolation errors affect both reflection and transmission measurements, primarily where the measured signal level is very low. Examples include reflection measurements of a well-matched DUT, and transmission measurements where the insertion loss of the DUT is large.

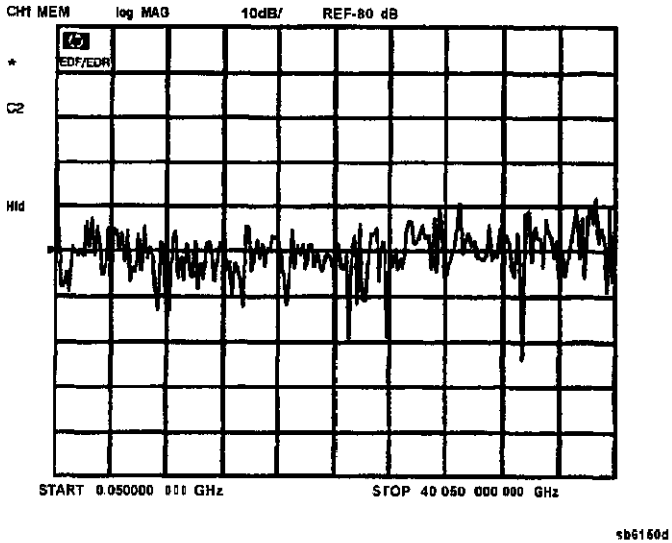


Figure 11-4. Typical EXF/EXR with 3 kHz Bandwidth

Load Match (ELF and ELR)

Load match is a measure of the impedance match of the test port that terminates the output of a 2-port device. The match of test port cables is included. Load match error terms are characterized by measuring the S11 and S22 responses of a "thru" configuration during the calibration procedure.

Significant System Components. Large variations in the forward or reverse load match error terms may indicate a bad "thru" cable or a poor connection of the cable to the test port.

Affected Measurements. The measurements most affected by load match errors are all transmission measurements, and reflection measurements of a low insertion

loss two-port device, such as an airline.

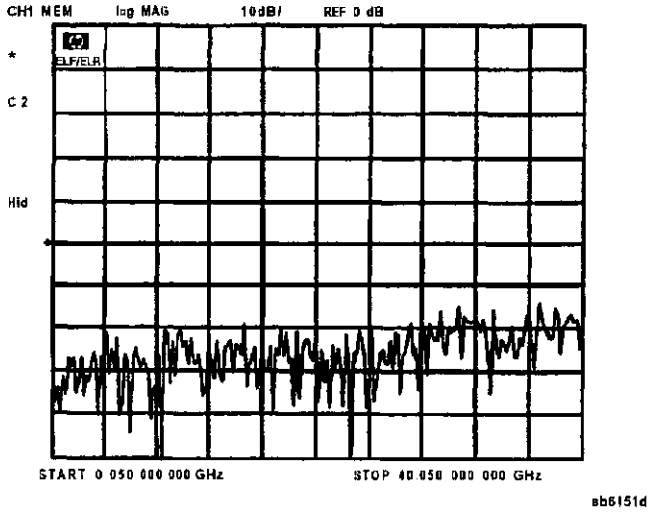


Figure 11-5. Typical ELF/ELR

Transmission Tracking (ETF and ETR)

Transmission tracking is the difference between the frequency response of the reference path (including R input) and the frequency response of the transmission test path (including A or B input) while measuring transmission. The response of the test port, cables is included. These terms are characterized by measuring the transmission (S21, S12) of the "thru" configuration during the measurement calibration. Note that coupler response is included in this error term. Typically transmission tracking appears as a slope of 0/-5 dB from 0.84 GHz to 40 GHz and a roll-off below 0.84 GHz, which is typically -3 dB at 500 MHz, -15 at 100 MHz, and -20 at 50 MHz.

Significant System Components. Large variations in this error term probably indicate a problem in the reference signal path (if both ETF and ETR are bad) or in the A or B input path. The "thru" cable also has an effect on transmission tracking.

Affected Measurements. All transmission measurements are affected by transmission tracking errors.

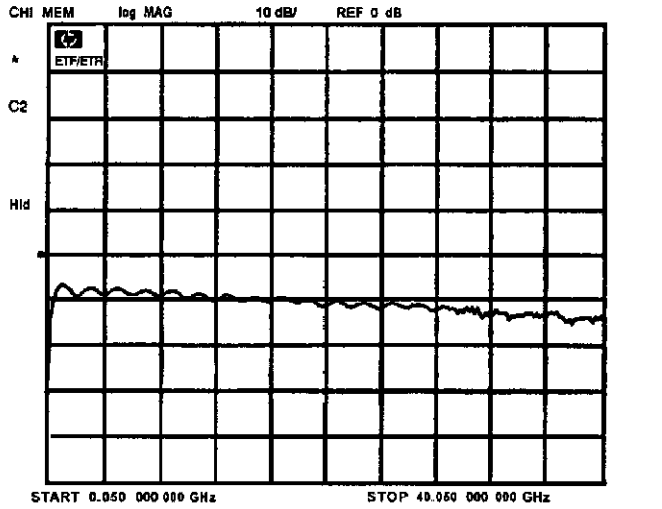


Figure 11-6. Typical ETF/ETR

Theory of Operation

Introduction

Theory of Operation provides a general description of the system, and operating theory of the network analyzer functional groups. Operation is explained to the assembly level only: component-level circuit theory is not provided. Simplified block diagrams illustrate the operation of each functional group. An overall block diagram is provided at the end of the section.

System Operation

The HP 8719D/20D/22D microwave network analyzers integrate a synthesized source, signal separation devices, a three-channel receiver for measurement of test device characteristics, and a large-screen display. Figure 12-1 is a simplified block diagram of the network analyzer system.

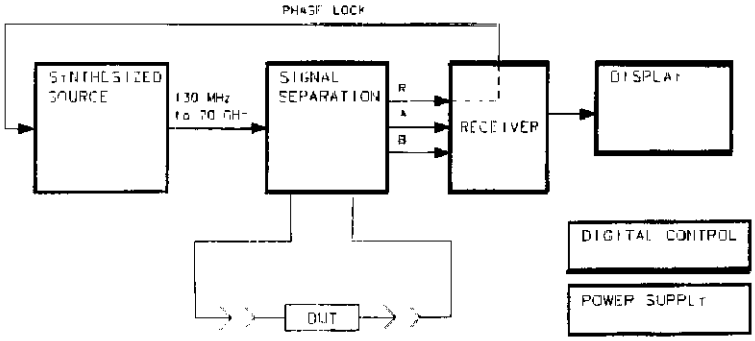


Figure 12-1. Simplified System Block Diagram

The built-in synthesized source of the analyzer generates a swept or CW (continuous wave) signal in the following ranges:

HP 8719D	HP 8720D	HP 8722D
50 MHz to 13.5 GHz	50 MHz to 20 GHz	50 MHz to 40 GHz

The source output power is leveled by an internal ALC (automatic leveling control) circuit, to a maximum level of +5 dBm (- 10 dBm, HP 8722D) at the front panel measurement ports. A portion of the source signal is routed to the R sampler in the receiver, and fed back to the source for phase lock.

The signal separation devices separate the source signal into a reference path and a test path. They provide attenuation for the source signal, RF path switching to allow forward and reverse measurements, and external connections for the DUT (device under test). The signal transmitted through or reflected from the DUT goes to the receiver for comparison with the reference signal.

The receiver converts the source signal to a 4 kHz IF (intermediate frequency) for signal processing, retaining both magnitude and phase characteristics. The IF is converted to digital signals, which are processed into magnitude and phase information. The processed and formatted data is finally routed to the display, and to the HP-IB for remote operation.

In addition to the analyzer, the system includes cables for interconnections, and calibration standards for accuracy enhanced measurements.

Functional Groups of the Analyzer

The operation of the analyzer is most logically described in five functional groups. Each group consists of several major assemblies, and performs a distinct function in the instrument. Some assemblies are related to more than one group, and in fact all the groups are to some extent interrelated and affect each other's performance.

Power Supply. The power supply functional group provides power for the other assemblies in the instrument.

Digital Control. The digital control group, which includes the front and rear

panels and the display, as well as the CPU, provides control to all assemblies in the network analyzer. The graphics signal processor (GSP) provides an interface between the CPU and the display.

Source. The source group supplies a phase-locked and leveled microwave signal to the device under test.

Signal Separation. The signal separation group performs the function of an S-parameter test set, dividing the source signal into a reference path and a test path, and providing connections to the device under test.

Receiver. The receiver group measures and processes the input signals for display

The following pages describe the operation of the assemblies within each of the functional groups.

Power Supply Theory

The power supply functional group consists of the A15 preregulator and the A8 post regulator. These two assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the analyzer. The A15 preregulator is enclosed in a casting at the rear of the instrument behind the display. It is connected to the A8 post regulator by a wire bus A15W1 Figure 12-2 is a simplified block diagram of the power supply group.

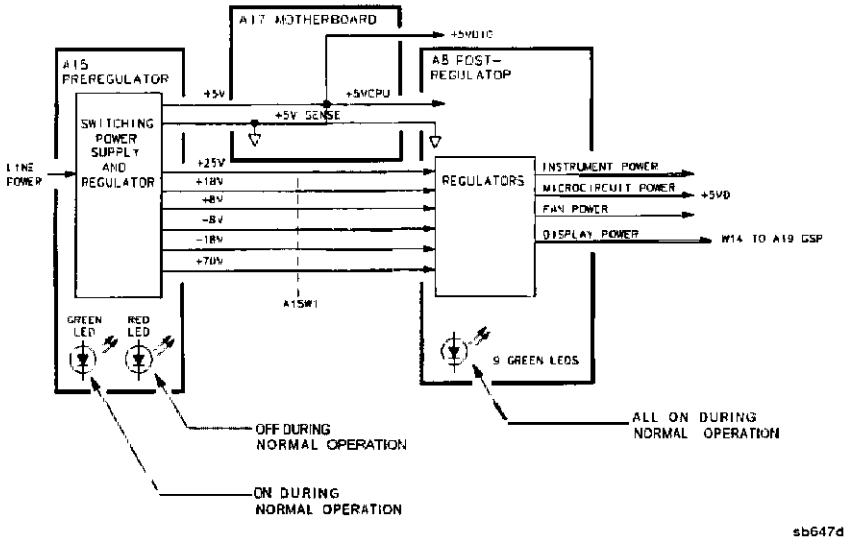


Figure 12-2. Power Supply Functional Group, Simplified Block Diagram

A 15 Preregulator

The A15 preregulator steps down and rectifies the line voltage. It provides a fully regulated +5 V digital supply, and several preregulated voltages that go to the A8 post regulator assembly for additional regulation.

The A15 preregulator assembly includes the line power module, a 60 kHz switching preregulator, and overvoltage protection for the +5 V digital supply. It provides LEDs, visible from the rear of the instrument, to indicate either normal or shutdown status.

Line Power Module

The line power module includes the line power switch, voltage selector switch, and main fuse. The line power switch is activated from the front panel. The voltage selector switch, accessible at the rear panel, adapts the analyzer to local line voltages of approximately 115 V or 230 V (with 350 VA maximum). The main fuse, which protects the input side of the preregulator against drawing too much line current, is also accessible at the rear panel. Refer to the *HP 8719D/20D/22D Network Analyzer Installation and Quick Start Guide* for line voltage tolerances and other power considerations.

Preregulated Voltages

The switching preregulator converts the line voltage to several DC voltages. The regulated +5V digital supply goes directly to the motherboard. The following partially regulated voltages are routed through A15W1 to the A8 post regulator for final regulation:

+70 V +25 V +18 V -18 V +8 V -8 V

Regulated + 5 V Digital Supply

The +5 VD supply is regulated by the control circuitry in the A15 preregulator. It goes directly to the motherboard, and from there to all assemblies requiring a low noise digital supply. A +5 V sense line returns from the motherboard to the A15 preregulator. The + 5 V CPU is derived from the + 5 VD in the A8 post regulator and goes directly to the A19 graphics system processor.

In order for the preregulator to function, the + 5 V digital supply must be loaded by one or more assemblies, and the +5 V sense line must be working. If not, the other preregulated voltages will not be correct.

Shutdown Indications: the Green LED and Red LED

The green LED is on in normal operation. It is off when line power is not connected, not switched on, or set too low, or if the line fuse has blown.

The red LED, which is off in normal operation, lights to indicate a fault in the +5 V supply. This may be an over/under line voltage, over line current, or overtemperature condition. Refer to the troubleshooting chapters for more information.

A8 Post Regulator

The A8 post regulator filters and regulates the DC voltages received from the A15 preregulator. It provides fusing and shutdown circuitry for individual voltage supplies. It distributes regulated constant voltages to individual assemblies throughout the instrument. It includes the overtemperature shutdown circuit, the variable fan speed circuit, and the air flow detector. Nine green LEDs provide status indications for the individual voltage supplies.

Refer to the Power Supply Block Diagram located at the end of Chapter 5, "Power Supply Troubleshooting", to see the voltages provided by the A8 post regulator.

Voltage Indications: the Green LEDs

The nine green LEDs along the top edge of the A8 assembly are on in normal operation, to indicate the correct, voltage is present in each supply. If they are off or flashing, a problem is indicated. The troubleshooting procedures later in this chapter detail the steps to trace the cause of the problem.

Shutdown Circuit

The shutdown circuit is triggered by overcurrent, overvoltage, undervoltage, or overtemperature. It protects the instrument by causing the regulated voltage supplies to be shut down. It also sends status messages to the A7 CPU to trigger warning messages on the analyzer display. The voltages that are not shut down are the + 5VD and + 5VCPU digital supplies from the preregulator, the fan supplies, and the display supplies. The shutdown circuit can be disabled momentarily for troubleshooting purposes by using a jumper to connect the SDIS line (A8TP4) to ground.

Variable Fan Circuit and Air Flow Detector

The fan power is derived directly from the + 18 V and -18 V supplies from the A15 preregulator. The fan is not fused, so that, it will continue to provide airflow and cooling when the instrument is otherwise disabled. If overheating occurs, the main instrument supplies are shut down and the fan runs at full speed. An overtemperature status message is sent. to the A7 CPU to initiate a warning message on the analyzer display. The fan also runs at full speed if the air flow detector senses a low output of air from the fan. (Full speed is normal at initial power on.)

Display Power

The A8 assembly supplies + 5VCPU and + 65 V (not used) to the A22 GSP interface board. The +5VCPU is routed to the A19 GSP where it is regulated to +3.3 V and sent to the display. The A19 GSP also controls and supplies power to the A20 backlight inverter. The voltages generated by the inverter are then routed to the display. Display power is not connected to the protective shutdown circuitry so that the A18 display assemblies can operate during troubleshooting when other supplies do not work.

Note **If blanking pulses from the A19 GSP are not present, then + 3.3 V will not be sent to the display.**

Digital Control Theory

The digital control functional group consists of the following assemblies:

- A1 front panel
- A2 front panel processor
- A7 CPU
- A10 digital IF
- A16 rear panel
- A18 display
- A19 GSP
- A20 Inverter

These assemblies combine to provide digital control for the entire analyzer. They provide math processing functions, as well as communications between the analyzer and an external controller and/or peripherals. Figure 6-1 is a block diagram of the digital control functional group.

A1 Front Panel

The A1 front panel assembly provides user interface with the analyzer. It includes the keyboard for local user inputs, and the front panel LEDs that indicate instrument status. The RPG (rotary pulse generator) is not electrically connected to the front panel, but provides user inputs directly to the front panel processor.

A2 Front Panel Processor

The A2 front panel processor detects and decodes user inputs from the front panel and the RPG, and transmits them to the CPU. It has the capability to interrupt the CPU to provide information updates. It controls the front panel LEDs that provide status information to the user.

A7 CPU/A10 Digital IF (firmware revisions 6.xx and below)

The A7 CPU assembly contains the main CPU (central processing unit), the digital signal processor, memory storage, and interconnect port interfaces. The main CPU is the master controller for the analyzer, including the other dedicated microprocessors. The memory includes EEPROM, RAM, EPROM, and ROM.

Data from the receiver is serially clocked into the A7 CPU assembly from the A10 digital IF. The data taking sequence is triggered either from the A14 fractional-N assembly, externally from the rear panel, or by software on the A7 assembly.

A7 CPU/A10 Digital IF (firmware revisions 7.xx and above)

The A7 CPU assembly contains the main CPU (central processing unit), the digital signal processor, memory storage, and interconnect port interfaces The main CPU is the master controller for the analyzer, including the other dedicated microprocessors. The memory includes EEPROM, DRAM, flash ROM, SRAM, and boot ROM.

Data from the receiver is serially clocked into the A7 CPU assembly from the A10 digital IF. The data taking sequence is triggered either from the A14 fractional-N assembly, externally from the rear panel, or by software on the A7 assembly.

Main CPU (firmware revisions 6.xx and below)

The main CPU is a 16-bit microprocessor that maintains digital control over the entire instrument through the instrument bus. The main CPU receives external control information from the front panel or HP-IB, and performs processing and formatting operations on the raw data in the main RAM. It controls the digital signal processor, the front panel processor, the display processor, and the interconnect port interfaces. In addition, when the analyzer is in the system controller mode, the main CPU controls peripheral devices through the peripheral port interfaces.

The main CPU has a dedicated EPROM that contains the operating system for instrument control. Front panel settings are stored in CMOS RAM, with a battery providing at least 5 years of backup storage when external power is off.

Main CPU (firmware revisions 7.xx and above)

The main CPU is a 32-bit microprocessor that maintains digital control over the entire instrument through the instrument bus. The main CPU receives external control information from the front panel or HP-IB, and performs processing and formatting operations on the raw data in the main RAM. It controls the digital signal processor, the front panel processor, the display processor, and the interconnect port interfaces. In addition, when the analyzer is in the system controller mode, the main CPU controls peripheral devices through the peripheral port interfaces.

The main CPU has a dedicated flash ROM that contains the operating system for instrument control Front panel settings are stored in SRAM, with a battery providing at least 5 years of backup storage when external power is off.

Main RAM

The main RAM (random access memory) is shared memory for the CPU and the digital signal processor. It stores the raw data received from the digital signal processor, while additional calculations are performed on it by the CPU. The CPU reads the resulting formatted data from the main RAM and converts it to GSP commands. It writes these commands to the GSP for output to the analyzer display.

EEPROM

EEPROM (electrically-erasable programmable read only memory) contains factory set correction constants unique to each instrument. These constants correct for hardware variations to maintain the highest measurement accuracy.

The correction constants can be updated by executing the routines in Chapter 3, "Adjustments and Correction Constants."

Digital Signal Processor

The digital signal processor receives the digitized data from the A10 digital IF. It computes discrete Fourier transforms to extract the complex phase and magnitude data from the 4 kHz IF signal. The resulting raw data is written into the main RAM.

A18 Display

The A18 display is an 8.4 inch LCD with associated drive circuitry. It receives a +3.3 V power supply from the A19 GSP, along with the voltage generated from the A20 backlight inverter. It receives the following signals from the A19 GSP:

- digital TTL horizontal sync
- digital TTL vertical sync
- blanking
- data clock
- digital TTL red video
- digital TTL green video
- digital TTL blue video

A19 GSP

The A19 graphics system processor provides an interface between the A7 CPU and the A18 display. The CPU (A7) converts the formatted data to GSP commands and writes it to the GSP. The GSP processes the data to obtain the necessary video signals and sends the signals to the A18 display. It also produces VGA compatible RGB output signals which are sent to the A22 GSP interface and then routed to the A16 rear panel. The assembly receives one power supply voltage from the A22 GSP interface: +5VCPU, which is used for processing and and supplying power to the A20 backlight inverter and the A18 display.

A20 Inverter

The A20 backlight inverter assembly supplies the ac voltage for the backlight tube in the A18 display assembly. This assembly takes the +5.16Vdc from the A1 mother board and converts it to approximately 380 Vac with 5 ma of current at 40 kHz. There are two control lines:

- Digital ON/OFF
- Analog Brightness
  100% intensity is 0 V
  50% intensity is 4.5 V

A16 Rear Panel

The A16 rear panel includes the following interfaces:

TEST SET I/O INTERCONNECT. This provides control signals and power to operate duplexer test adapters.

EXT REF. This allows for a frequency reference signal input that can phase lock the analyzer to an external frequency standard for increased frequency accuracy.

The analyzer automatically enables the external frequency reference feature when a signal is connected to this input. When the signal is removed, the analyzer automatically switches back to its internal frequency reference.

10 MHZ PRECISION REFERENCE. (Option 1D5) This output is connected to the EXT REF (described above) to improve the frequency accuracy of the analyzer.

AUX INPUT. This allows for a dc or ac voltage input from an external signal source, such as a detector or function generator, which you can then measure, using the S-parameter menu. (You can also use this connector as an analog output in service routines.)

EXT AM. This allows for an external analog signal input that is applied to the ALC circuitry of the analyzer's source. This input analog signal amplitude modulates the RF output signal.

EXT TRIG. This allows connection of an external negative-going TTL-compatible signal that will trigger a measurement sweep. The trigger can be set to external through softkey functions.

TEST SEQ. This outputs a TTL signal that can be programmed in a test sequence to be high or low, or pulse (10 μseconds) high or low at the end of a sweep for a robotic part handler interface.

LIMIT TEST. This outputs a TTL signal of the limit test results as follows:

Pass: TTL high

Fail: TTL low

VGA OUTPUT. This provides a video output of the analyzer display that is capable of running a PC VGA monitor

Source Group Theory

The source functional group produces a stable output signal by phase locking a YIG oscillator to a synthesized VCO (voltage controlled oscillator). The full frequency range of the source is generated in subsweeps by harmonic mixing.

The output is a swept or CW signal with a maximum leveled power of +5 dBm (-10 dBm, HP 8722D) at the front panel measurement ports (minimum -65 dBm). Figure 12-3 illustrates the operation of the source functional group.

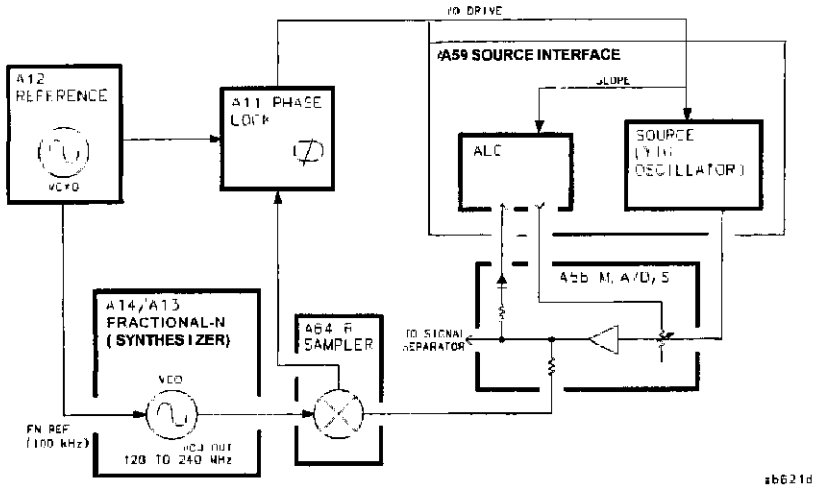


Figure 12-3. Source Functional Group, Simplified Block Diagram

The subsweep sequence takes place in the following steps. The paragraphs below describe the details of this process, and provide additional information on the assemblies in the source group.

1. The source is pretuned low. The source signal (SOURCE OUT) is fed to the R sampler.
2. A signal (VCO OUT) is generated by the VCO in the fractional-N synthesizer.
3. A comb of harmonics (1st LO) is produced in the pulse generator.
4. A synthesizer harmonic (1st LO) and the source signal (SOURCE OUT) are mixed in the sampler. A difference frequency (1st IF) is generated.
5. The 1st IF signal from the R sampler is fed back and compared to a reference. A tune current is generated.
6. The tune current is used to set the frequency of the source YIG oscillator.
7. Phase lock is acquired and a synthesized subsweep is generated. The source tracks the synthesizer

Source Pretune

The pretune DAC (digital-to-analog converter) in the All phase lock assembly sets the source YIG oscillator frequency to approximately 2.4 GHz This signal (SOURCE OUT) goes to the R sampler assembly

A 14/A 13 Fractional-N Synthesizer

The A14/A13 fractional-N assemblies comprise the synthesizer. The source feedback circuit phase locks the YIG oscillator to the synthesizer output signal as explained below under "A11 Phase Lock: Comparing Phase and Frequency."

The VCO in the Al4 fractional-N (digital) assembly generates a swept or CW signal in the range of 60 to 240 MHz, such that a harmonic is 10 MHz above the desired start frequency. This is divided down and phase locked (in the Al3 assembly) to a 100 kHz signal FN REF from the Al2 reference. A programmable divider is set to some number, N, such that the integer part of the expression FVCO/N is equal to 100 kHz. To achieve frequencies between integer multiples of the reference, the divider is programmed to divide by N part of the time and by N+ 1 part of the time. The ratio of the divisions yields an average equal to the desired fractional frequency. API (analog phase interpolator) current sources in the Al3 assembly correct for phase errors caused by the averaging. The resulting synthesized signal goes to the pulse generator.

A52 Pulse Generator: the Harmonic Comb

The signal from the synthesizer drives a step recovery diode (SRD) in the A52 pulse generator assembly. The SRD generates a comb of harmonic multiples (1st LO) of the VCO frequency, which goes to the samplers. One of the harmonics is 10 MHz above the desired start frequency.

A64 R Sampler: Down-Converting the Signals

The A64 assembly is part of the receiver functional group. It is also included here because it is an integral part of the source phase locking scheme. In the R sampler, the 1st LO signal from the pulse generator is mixed with the SOURCE OUT signal from the source The difference IF (intermediate frequency) produced is nominally 10 MHz. For phase locking, part of this IF signal is routed back to the All phase lock assembly. (Additional information on the sampler assemblies is provided in "Receiver Theory.")

All Phase Lock: Comparing Phase and Frequency

The 10 MHz 1st IF signal from the A64 sampler is fed back to the All phase lock assembly In All it is amplified, limited, and filtered to produce a 10 MHz square wave. This is divided down to 1 MHz, then applied to a phase/frequency detector that compares it to a crystal controlled 1 MHz signal (PL REF) from the A12 reference assembly (see "A12 Reference: the Crystal Reference Frequencies," below). Any phase or frequency difference between these two signals produces a proportional DC voltage.

Tuning the YIG Oscillator

The output of the phase/frequency detector is filtered to remove any 1 MHz feedthrough, and fed to an integrator. The output of the integrator is converted to a tune current. This brings the appropriate YIG oscillator closer to the desired frequency, which in turn reduces the phase/frequency detector output voltage. When the voltage is reduced to zero, and the divided-down 1st IF frequency is equal to the 1 MHz reference frequency PL REF, phase lock is achieved.

Phase Locked Sweep

When the source is phase locked to the synthesizer at the start frequency, the synthesizer starts to sweep. The phase-locked loop forces the source to track the synthesizer, maintaining a constant 10 MHz 1st IF signal.

The full sweep is generated in a series of subsweeps, by phase locking the source signal to the harmonic multiples of the synthesizer. At the transitions between subsweeps, phase lock is broken, the source is held at this frequency. Table 12-1 lists the subsweep frequencies from the synthesizer and the source.

Table 12-1. Subsweep Frequencies

Band	Synthesizer (MHz)	Harmonic Number (N)	Source (MHz) Frequency
Low	60 - 120	1	50 - 110
	120 - 240	1	110-230
	120 240	2	230 - 470
	160 - 236	3	470 698
	141.6- 236	5	698 - 1170
	147.6 - 236	8	1170 - 1878
	157.3 - 213.3	12	1878 - 2550
High Mid (HP 8722D)	128 - 236	20	2550 - 4710
	131.1 - 220/6	36	4710 - 8256
	142.5 - 234	58	8256 - 13562
	159.7 - 235.4	85	13562 - 20000
High (HP 87221D)	178.7 223.3	112	20000 - 25000
	148.9 238.2	168	25000 - 40000

A12 Reference: the Crystal Reference Frequencies

This assembly provides stable reference frequencies to the rest of the instrument by dividing down the output of a 40 MHz VCXO (voltage-controlled crystal oscillator). One of the divided-down signals is the 100 kHz FN REF for phase locking the synthesizer signal in A13. Another is the 1 MHz main phase-locked loop reference signal PL REF that goes to the phase comparator in All. (The 2nd LO signal and the timing signal for the A10 digital IF assembly are explained in "Receiver Theory. ") The EXT REF rear panel input provides the option of using an external reference with a frequency of 1, 2, 5, or 10 MHz, instead of the internal 40 MHz VCXO.

Source Block: The YIG Oscillator Signals

The source block includes two YIG oscillators and a 3.8 GHz fixed oscillator. The outputs of these oscillators produce the source signal. In phase-locked operation, this signal tracks the stable output of the synthesizer. Figure 12-4 illustrates the assemblies in the source block.

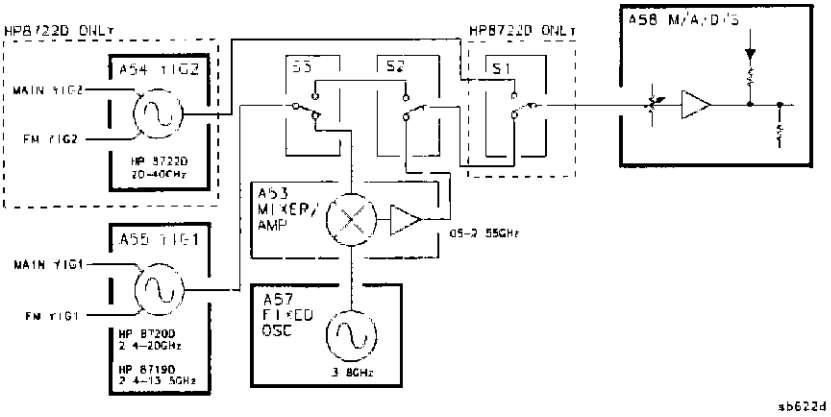


Figure 12-4. Simplified Diagram of the Source Block

The YIG oscillator has a main coil and an FM coil. These are analogous to the woofer and the tweeter in a stereo speaker. the woofer reproduces low frequencies and the tweeter reproduces high frequencies. Similarly in the YIG oscillator, the main coil allows large, slow changes in frequency but cannot respond to high frequency deviations, which are sent to the faster-acting FM coils.

The tune current from the All phase lock assembly splits into two paths. One path is lowpass filtered, removing high frequency components, and goes to the YIG main coil; the other path is highpass filtered, removing low frequency components, and goes to the YIG FM coils. The filters are matched in stop-band response, such that one picks up where the other leaves off.

The full YIG oscillator frequency range is achieved in two bands:

Band	Frequency Range
Low	50 MHz to 2.55 GHz
High Mid (HP 8722D)	2.55 GHz to 20.0 GHz
High (HP 8722D)	20 GHz to 40 GHz

In the low band, the 2.4 to 20 GHz output of YIG1 and the fixed 3.8 GHz output of the A57 fixed oscillator are mixed in the A53 mixer/amplifier assembly. In this band, S2 and S3 switch A53 into the circuit.

The high band (mid band, HP 8722D) uses the output of YIG1.

The high band (HP 8722D) uses the output of YIG2.

In the A58 M/A/D/S microcircuit, the YIG oscillator signal is modulated by the ALC OUT signal (explained below) to provide power control and leveling.

ALC: Automatic Leveling Control

A portion of the source output is detected in the M/A/D/S and sent back to the source Interface Board ALC circuit. This circuit generates a control signal which is sent to the modulator in the M/A/D/S to control the power. The tune voltage from the main coil drive is used to change the source amplitude as a function of frequency, thus compensating the source for losses in the transfer switch, bias tees, and couplers.

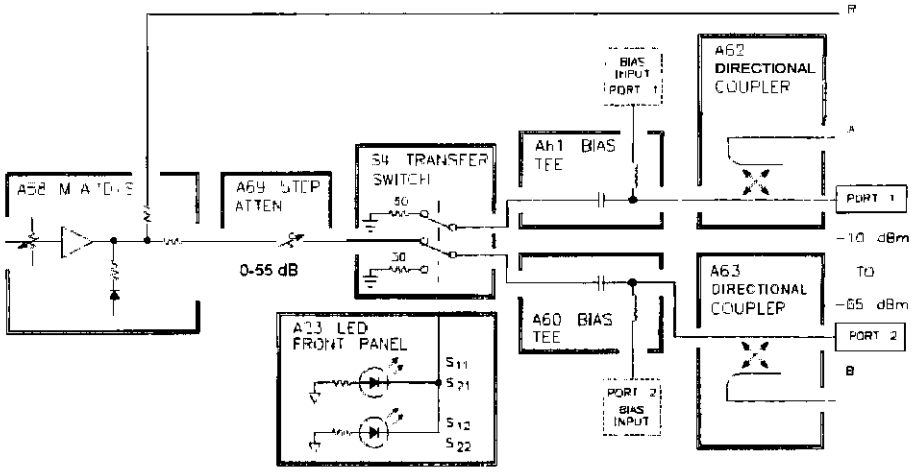


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Figure 12-5. Signal Separation, Simplified Block Diagram

A58 M/A/D/S Modulator, Amplifier, Detector, Splitter

The M/A/D/S microcircuit accomplishes four separate functions:

The modulator controls the output power proportionally to the signal produced by the ALC circuit on the source Interface board.

The amplifier provides up to + 30 dB of amplification that will allow up to + 5 dBm (-10 dBm, HP 8722D) to be output from the test port.

The detector outputs a voltage that is proportional to the RF power out of the amplifier. This voltage is used by the ALC circuit on the source Interface board.

The power source divides the source signal into two parts. One signal is routed directly to the A64 R sampler and the other is sent through the A69 step attenuator, S4 transfer switch, A60 and A61 bias tees, A62/A63 directional couplers and to the test ports.

The M/A/D/S microcircuit is controlled by the ALC circuitry on the source interface board. The CPU provides fine control of the test port power for applications such as power sweep.

Option 400 A58 M/A/D, and A74 Switch Splitter

The M/A/D (Modulator/Amplifier/Detector) microcircuit accomplishes three functions:

The modulator controls the output power proportionally to the signal produced by the ALC circuit on the source interface board.

The amplifier can provide + 30 dB of amplification for test port output power levels up to + 5 dBm for HP 8719D/20D (-10 dBm for HP 8722D).

The detector outputs a voltage that is proportional to the RF power out of the amplifier. The voltage is used by the ALC circuit on the source interface board.

The switch splitter (A74) divides three inputs:

- a path routed directly to A64 (R1 sampler)
- a path routed directly to the A67 (R2 sampler)
- a path switched to the appropriate output port (through A70/71 step attenuators, A60/61 bias tees, and A62/63 directional couplers)

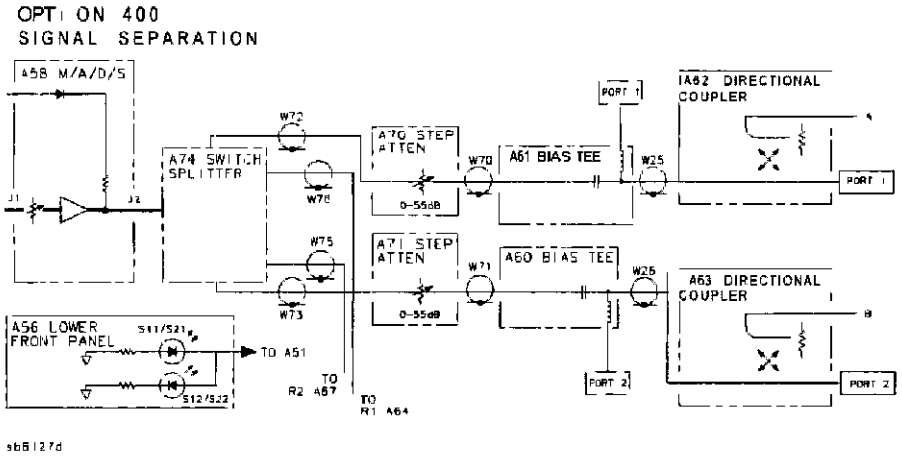

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Figure 12-6. Option 400 Signal Separation

A69 Step Attenuator

The step attenuator provides coarse power control for the source signal. It is an electro-mechanical attenuator, controlled by the A7 CPU, that provides 0 to 55 dB of attenuation in 5 dB steps. It adjusts the power level to the DUT without changing the level of the incident power in the reference path.

S4 Transfer Switch

The output of the step attenuator is fed into the S4 transfer switch. This is a solid-state switch. It switches between the port 1 and port 2 measurement paths, automatically enabling alternate forward and reverse measurements. In addition, S4 provides an internal termination for the measurement port that is inactive.

A56 Lower Front Panel Assembly

LEDs on the lower front panel indicate the status of the transfer switch.

A60 and A61 DC Bias Tees

The DC bias tees provide a means of biasing active devices with an external DC voltage connected to the rear panel DC BIAS CONNECT ports. The DC voltage is applied directly to the center conductor of the test port connectors. A blocking capacitor ensures that the bias current goes only to the device under test, and not back into the source. Likewise, an inductor in the bias path prevents RF from being imposed on the external DC supply.

A62 and A63 Directional Couplers

The test signal goes into the through-line arm of the couplers, and from there to the test ports and the device under test. The coupled arm of the couplers carries the signal reflected from or transmitted through the device under test to the receiver for measurement. The coupling coefficient of the directional couplers is nominally 20 dB (40 dB at 50 MHz).

Receiver Theory

The receiver measures and processes the input signals into digital information for display. Figure 12-7 is a simplified block diagram of the receiver functional group. The A12 reference assembly, which is part of the source group, is also included in the illustration to show how the 2nd LO signal is derived.

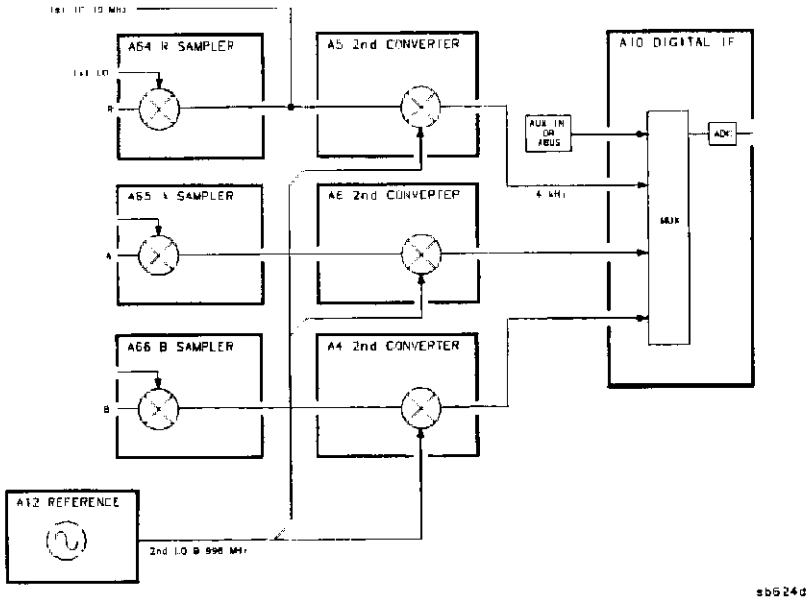


Figure 12-7. Receiver Functional Group, Simplified Block Diagram

Samplers and Second Converters

Each input signal goes to one of three identical pairs of sampler and second converter assemblies (R, A, and R) that down-convert the signals to a fixed 4 kHz 2nd IF with magnitude and phase corresponding to the input.

The 1st LO Signal is a comb of harmonics of the synthesizer signal, produced by a step recovery diode in the A52 pulse generator. Refer to "Source Group Theory" for details.

A64/A65/A66 (A67 Option 400) Samplers. The signal from the source is mixed with the 1st LO harmonics in the samplers One of the harmonic signals is 10 MHz above the desired frequency. The mixing products are filtered, leaving only the difference between that harmonic and the source frequency: this fixed 10 MHz signal is the 1st IF (Fir = N x FVCO – F_S, where N is the harmonic number). Part of the 1st IF signal from the R sampler is fed back to the A11 phase lock assembly to complete the source phase-locked loop. The 1st IF from all three samplers goes to the corresponding second converters. The A67 sampler is only used in Option 400 instruments.

2nd LO Signal. The stable 2nd LO signal is produced in the A12 reference assembly by phase locking and mixing a 39.984 MHz VCO with the 40 MHz VCXO to derive a difference of 16 kHz This is compared to a 16 kHz reference produced by dividing 40 MHz by 2500. The phase-locked output of the 39.984 MHz oscillator is divided by 4 to provide the 9.996 MHz 2nd LO.

A4/A5/A6 Second Converters. The 1st IF and the 2nd LO are mixed in the second converter. The resulting difference frequency is a constant 4 kHz 2nd IF signal that retains the amplitude and phase characteristics of the measured signal. The 2nd IF signals from all three second converter assemblies are input to the A10 digital IF assembly.

A10 Digital IF

In this assembly, the 2nd IF signals from the A and B second converters go through a gain stage. Signals lower than -30 dB on these two signal paths are amplified by 24 dB to ensure that they can be detected by the ADC (analog-to-digital converter). For troubleshooting purposes, the gain can be forced on or off using the service menus (refer to "Receiver Troubleshooting"). The R path signal is fixed at a level high enough to maintain phase lock, and therefore requires no amplification.

All three signals are sampled at a 16 kHz rate set by a divided-down 4 MHz clock pulse from the A12 reference assembly. The signals are sequentially multiplexed into the ADC, where they are converted to digital form. The ADC conversions are triggered by timing signals from the CPU or the synthesizer, or an external signal at the rear panel EXT TRIG connector The digitized data is serially clocked into the A7 CPU assembly to be processed into magnitude and phase data.

The processed and formatted data is finally routed to the display, and to the HP-IB for remote operation. Refer to "Digital Control Theory" in this section and to Data Processing in the first chapter of the Reference for more information on signal processing.

An additional input to the A10 assembly is the analog bus (ABUS), a built-in service tool for testing analog circuits within the instrument. This is a single multiplexed line that networks analog nodes throughout the instrument, or monitors an external input at the rear panel AUX INPUT connector. It is controlled by the CPU, and used like an oscilloscope or frequency counter to make internal voltage and frequency measurements.

Replaceable Parts

This chapter contains information for ordering replacement parts for the HP 8719D/8720D/8722D network analyzer. Replaceable parts include the following:

- major assemblies
- cables
- hardware

In general, parts of major assemblies are not listed Refer to Table 13-2 at the back of this chapter to help interpret part descriptions in the replaceable parts lists that follow.

Replacing an assembly

The following steps show the sequence to replace an assembly in an HP 8719D/8720D/8722D network analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Rebuilt-Exchange Assemblies

Under the rebuilt-exchange assembly program, certain factory-repaired and tested modules (assemblies) are available on a trade-in basis. These assemblies are offered for lower cost than a new assembly, but meet all factory specifications required of a new assembly.

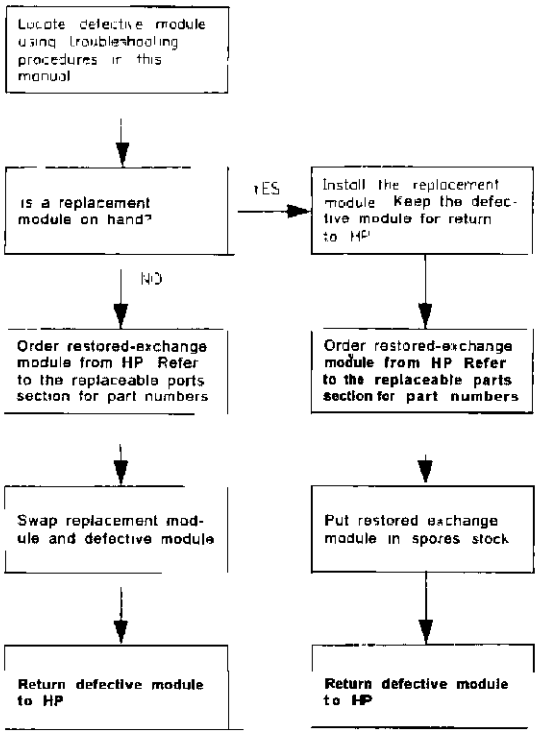
The defective assembly must be returned for credit under the terms of the rebuilt-exchange assembly program. Any spare assembly stock desired should be ordered using the new assembly part number. Figure 13-1 illustrates the module exchange procedure. "Major Assemblies, Top" and "Major Assemblies, Bottom" list all major assemblies, including those that can be replaced on an exchange basis.

Ordering Information

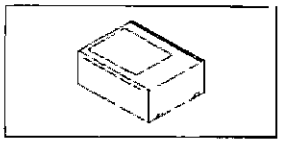
To order a part listed in the replaceable parts lists, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The Hewlett-Packard Sales and Service Offices table is located in Chapter 15.

To order a part that is not listed in the replaceable parts lists, include the instrument model number, complete instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service

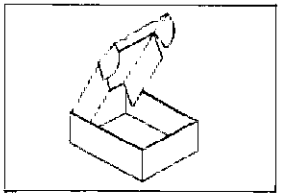


A.



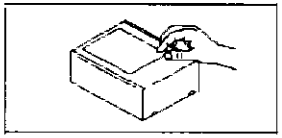
Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains: Exchange assembly failure report Return address label

B



Open box carefully-it will be **used to return defective module to HP. Complete failure report. Place it and defective module in box. Be sure to remove enclosed return address label.**

C.



Seal box with tape. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label, instead address box to the nearest HP office.

*HP pays postage on boxes mailed in U.S.A.

sg613d

Figure 13-1. Module Exchange Procedure

Replaceable Part Listings

The following pages list the replacement part numbers and descriptions for the HP 8719D/8720D/8722D Network Analyzer. Illustrations with reference designators are provided to help identify and locate the part needed. The parts lists are organized into the following categories:

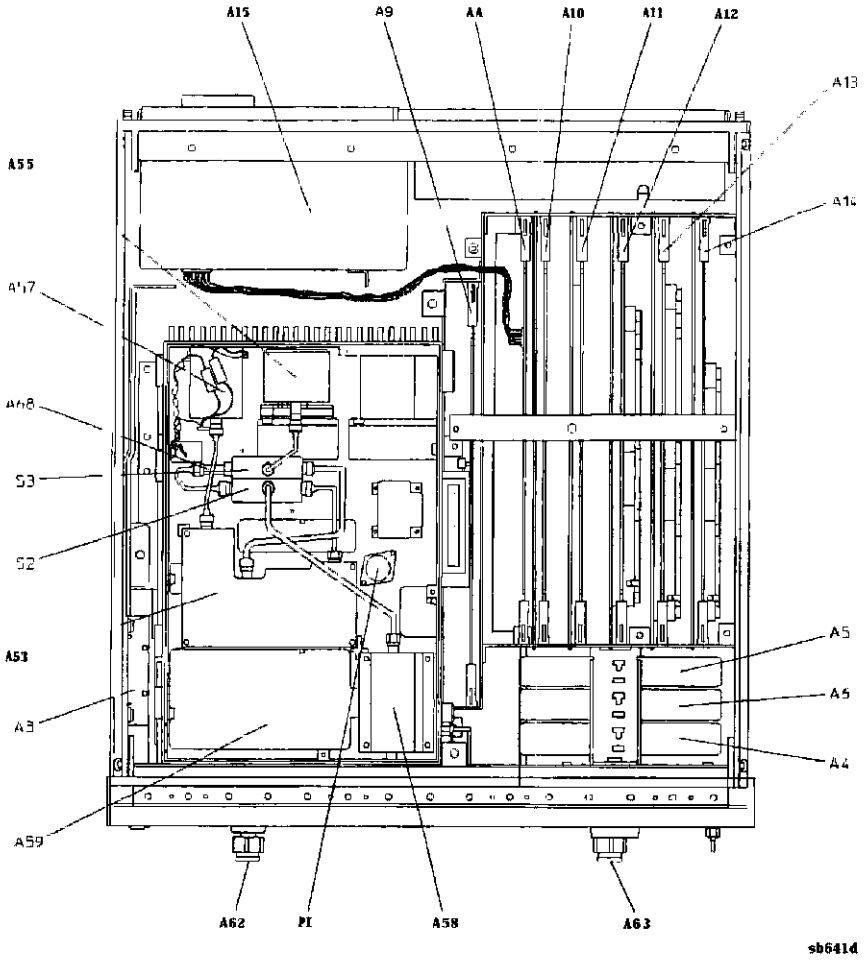
- Major Assemblies, Top
- Major Assemblies, Bottom
- Cables, Top
- Cables, Bottom
- Cables, Front
- Cables, Rear
- Front Panel, Outside
- Front Panel, Inside
- Rear Panel
- Rear Panel, Option 1D5
- Hardware, Top
- Hardware, Bottom
- Hardware, Front
- Hardware, Preregulator
- Chassis Parts, Outside
- Chassis Parts, Inside
- Miscellaneous

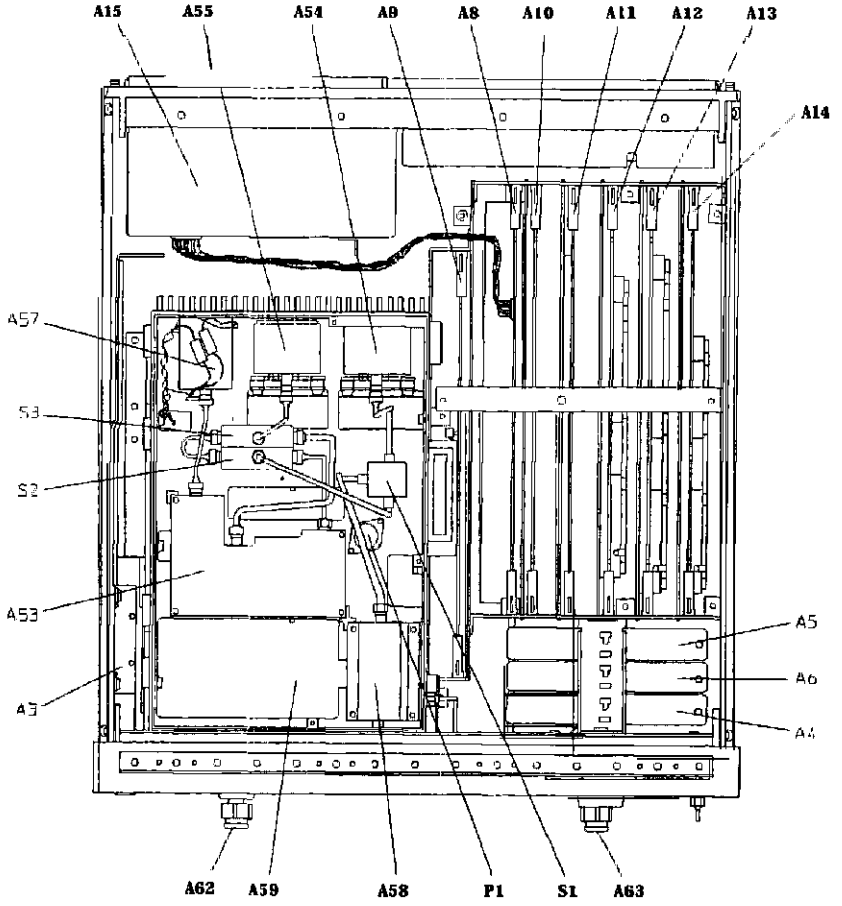
Major Assemblies, Top

Ref Desig	Option	HP Part Number	Qty	Description
A1				NOT SHOWN (see "Front Panel Assembly, Inside")
A2				NOT SHOWN (see "Front Panel Assembly, Inside")
A3		08720-60190	1	DISK DRIVE ASSY
A4 A5 A6		08720-60156	1	ASSY-SECOND CONVERTER
A7				NOT SHOWN (see "Major Assemblies, Bottom")
A8*		08722-60011	1	BD ASSY-POST REGULATOR (8719D/8720D)
A8*		08722-69011	1	BD ASSY-POST REGULATOR (REBUILT-EXCHANGE) (8719D/8720D)
A8*		08722-60011	1	BD ASSY-POST REGULATOR (8722D)
A9		08720-60129	1	BD ASSY-SOURCE CONTROL
A10		08753-60095	1	BD ASSY-DIGITAL IF
A10		08753-69096	1	BD ASSY-DIGITAL IF (REBUILT-EXCHANGE)
A11		08720-60181	1	BD ASSY-PHASE LOCK
A12		08720-60252	1	BD ASSY-REFERENCE
A12		08720-69252	1	BD ASSY-REFERENCE (REBUILT-EXCHANGE)
A13		08720-60049	1	BD ASSY-FRAC N ANALOG
A13		08720-69049	1	BD ASSY-FRAC N ANAMG (REBUILT-EXCHANGE)
A14		08720-60179	1	BD ASSY-FRAC N DIGITAL
A14		08720-69179	1	BD ASSY-FRAC N DIGITAL (REBUILT-EXCHANGE)
A15		08753-60098	1	ASSY-PREREGULATOR
A15		08753-69098	1	ASSY-PREREGULATOR (REBUILT-EXCHANGE)
A16				NOT SHOWN (see "Rear Panel Assembly")
A17				NOT SHOWN (see "Chassis Parts, Inside")
A18				NOT SHOWN (see "Front Panel Assembly, Inside")
A19				NOT SHOWN (see "Cables, Front")
A20				NOT SHOWN (see "Front Panel Assembly, Inside")
A22				NOT SHOWN (see "Cables, Front")
A26	1D5			NOT SHOWN (see "Rear Panel Assembly, Option 1D5")
A61				NOT SHOWN (see "Major Assemblies, Bottom")
A63		5086-7583	1	ASSY-LOW BAND
A63		5086-6583	1	ASSY-LOW BAND (REBUILT-EXCHANGE)
A64		08722-60013	1	ASSY-YIG OSCILLATOR 20 GHz TO 40 GHZ (8722D)
A66		08720-60082	1	ASSY-YIG OSCILLATOR2 4 GHZ TO 20 GHZ (8720D/8722D)
A65		08719-60009	1	ASSY-YIG OSCILLATOR 2 4 GHZ TO 13 6 GHZ (8719D)

Ref Desig	Option	HP Part Number	Qty	Description
A56				NOT SHOWN (see 'Cables, Front')
A57		08720-60073	1	ASSY-FIXED OSCILLATOR
A58		5086-7519	1	ASSY-M/A/D/S (8719D/8720D)
A58		50866519	1	ASSY-M/A/D/S (8719D/8720D) (REBUILT EXCHANGE)
A58	004	5086-7974	1	ASSY-M/A/D2 98719D/8720D)
A58	004	5086-6974	1	ASSY-M/A/D/S2 (8719D/8720D) (REBUILT-EXCHANGE)
A58		5086-7615	1	ASSY-SUPER M/A/D/S (8722D)
A58		5086-7615	1	ASSY-SUPER M/A/D/S (8722D) (REBUILT-EXCHANGE)
A58	400	5086-7980	1	ASSY-M/A/D/S2 (8722D)
A58	400	5086-6980	1	ASSY-M/A/D/S2 (8722D) (REBUILT-EXCHANGE)
A59		08720-60139	1	BD ASSY-SOURCE INTERFACE
A62 63		60867968	2	ASSY-DIRECTIONAL COUPLER 8719D/8720D)
A62, 63		5086-7518	2	ASSY-DIRECTIONAL COUPLER (8722D)
A68		0955-0462	1	ATTENUATOR 6 DB (8719D/8720D)
A72, A73				NOT SHOWN (see 'Cables, Front')
A75				NOT SHOWN (see 'Cables, Front')
A76				NOT SHOWN (see 'Cables, Front')
P1		1826-0423	1	IC-VOLTAGE REGULATOR
S1		5086-7589	1	ASSY-SWITCH 40 GHZ (8722D)
S2,S3		08415-60067	1	ASSY-MICROWAVE SWITCH

* For fuse part numbers on the A8 Post Regulator refer to Table 13-1 in this chapter.


A15
A9
A4
A10
A11
A12
A13
A55
A17
A8
S3
S2
A53
A3
A59
A5
A5
A4
A62
P1
A58
A63
sb641d


A15
A55
A54
A9
A8
A10
A11
A12
A13
A14
A57
S3
S2
A53
A3
A5
A6
A4
A62
A59
A58
P1
S1
A63

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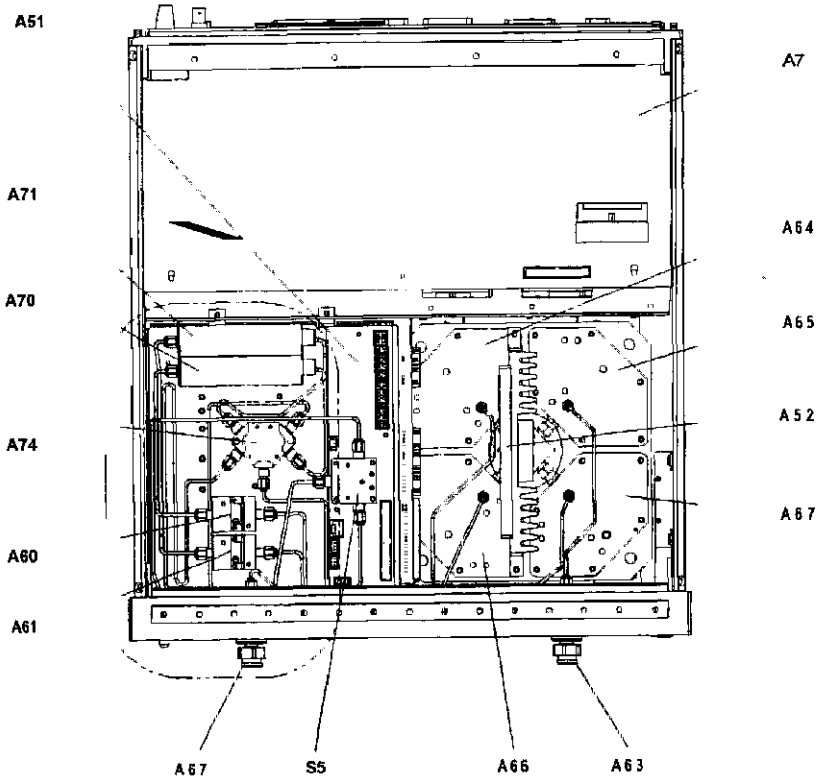
Major Assemblies, Bottom

Ref. Desig.	Option	HP Part Number	Qty	Description
A7		08720-60140	1	BD ASSY-CPU (F/W REV 6 XX AND BELOW)
A7		08720-6025	1	CPU REPAIR KIT (F/W REV 7 XX AND ABOVE)
A7		08720-69253	1	CPU REPAIR KIT (F/W REV 7 XX AND ABOVE) (REBUILT-EXCHANGE)
A7BT1		1420-0338	1	BATTERY-LITHIUM 3 V 1 2AH
A51		08720-60137	1	BD ASSY-TEST INTERFACE
A51	400	08720 60178	1	BD ASSY TEST INTERFACE
A52		5086-7456	1	ASSY-PULSE GENERATOR
A52		5086 6456	1	ASSY-PULSE GENERATOR (REBUILT-EXCHANGE)
A60,61		5086-7458	1	BIAS TEE (8719D/8720D)
A60.61		5086-6458	1	BIAS TEE (8719D/8720D) (REBUILT-EXCHANGE)
A60.61		6086-7484	1	BIAS TEE (8722D)
A60.61		5086 6484	1	BIAS TEE (8722D) (REBUILT-EXCHANGE)
A62.63		5086-7968	2	ASSY-DIRECTIONAL COUPLER (8719D/8720D)
A62.63		5086 6968	2	ASSY-DIRECTIONAL COUPLER (8719D/8720D) (REBUILT-EXCHANGE)
A62,63		6086-7518	2	ASSY-DIRECTIONAL COUPLER (8722D)
A62,63		5086 6518	2	ASSY-DIRECTIONAL COUPLER (8722D) (REBUILT-EXCHANGE)
A64,A65, A66,A67		5086-7614	1	ASSY-SAMPLER
A64,A65, A66,A67		5086-6614	1	ASSY-SAMPLER (REBUILT-EXCHANGE)
A69	ALL BUT 085,400	3332160060	1	ATTENUATOR 0-55 DB
A69	085,400	33326 60006	1	ATTENUATOR 0-55 DB
A70,A71, A75,A76		33326-60006	1	ATTENUATOR 0-55 DB
A74	400,089	5086-7975	1	ASSY-SWITCH SPLITTER (8719D/8720D)
A74	400,089	5086-6975	1	ASSY-SWITCH SPLITTER (8719D/8720D) (REBUILT-EXCHANGE)
A74	400,089	5087-7002	1	ASSY-SWITCH SPLITTER (8722D)
A74	400,089	5087-6002	1	ASSY-SWITCH SPLITTER (8722D) (REBUILT-EXCHANGE)
S4		5086-7642	1	ASSY-TRANSFER SWITCH SOLID STATE (8719D/8720D)
S4	007	08720-60006	1	ASSY-TRANSFER SWITCH (8719D/8720D)
S4	007	08722-60015	1	ASSY-TRANSFER SWITCH (8722D)
S4	007	08722-69015	1	ASSY-TRANSFER SWITCH (8722D) (REBUILT-EXCHANGE)
S4		85331-60033	1	ASSY-TRANSFER SWITCH (8722D)
S5	089	5086 7589	1	SWITCH



HP 8722D OPTIONS 400, 089
HP 8719D/20D OPTIONS 400, 089

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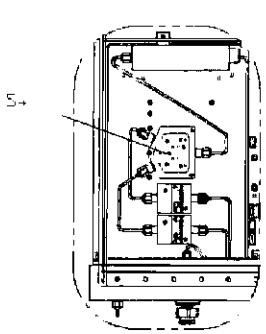
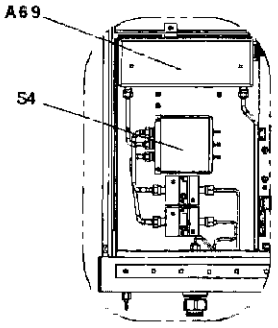
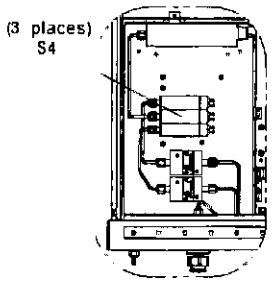


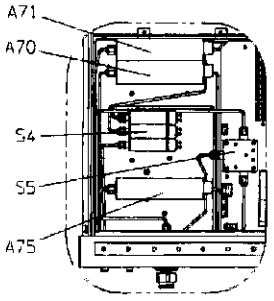
HP 8722D
STANDARD



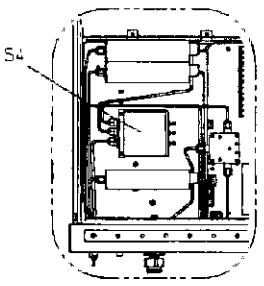
HP 8719D/20D
STANDARD OPTION 007



HP 8722D
OPTION 007



HP 8722D
OPTIONS 085, 089



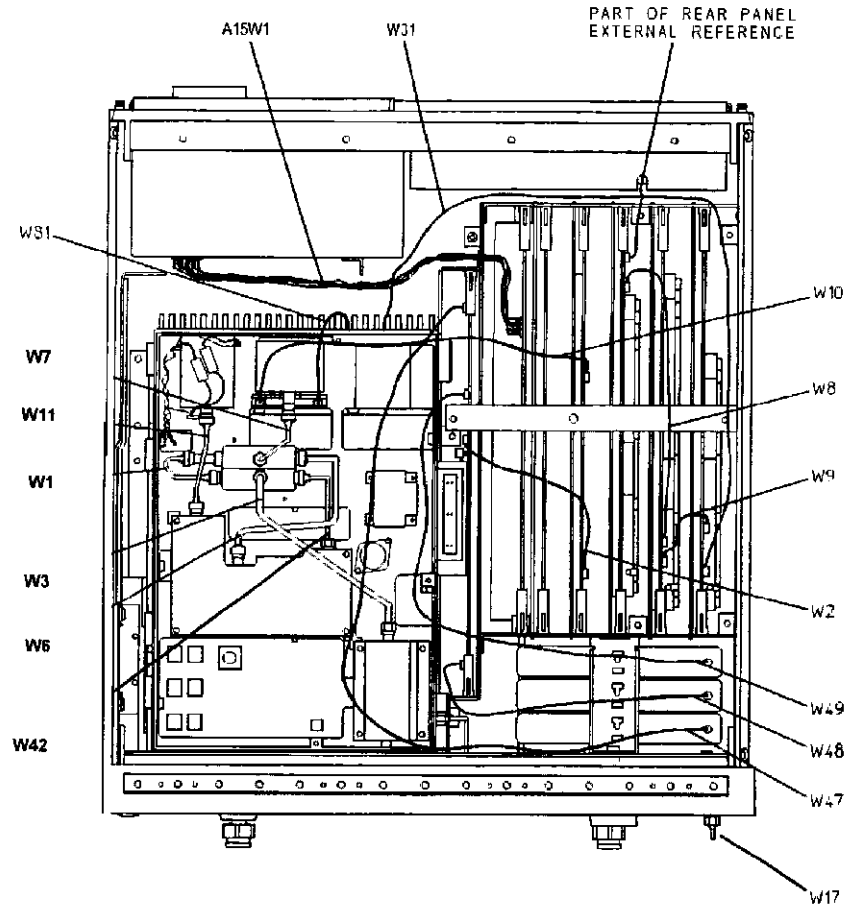
HP 8719D/20D
OPTIONS 085, 089

sb6140d

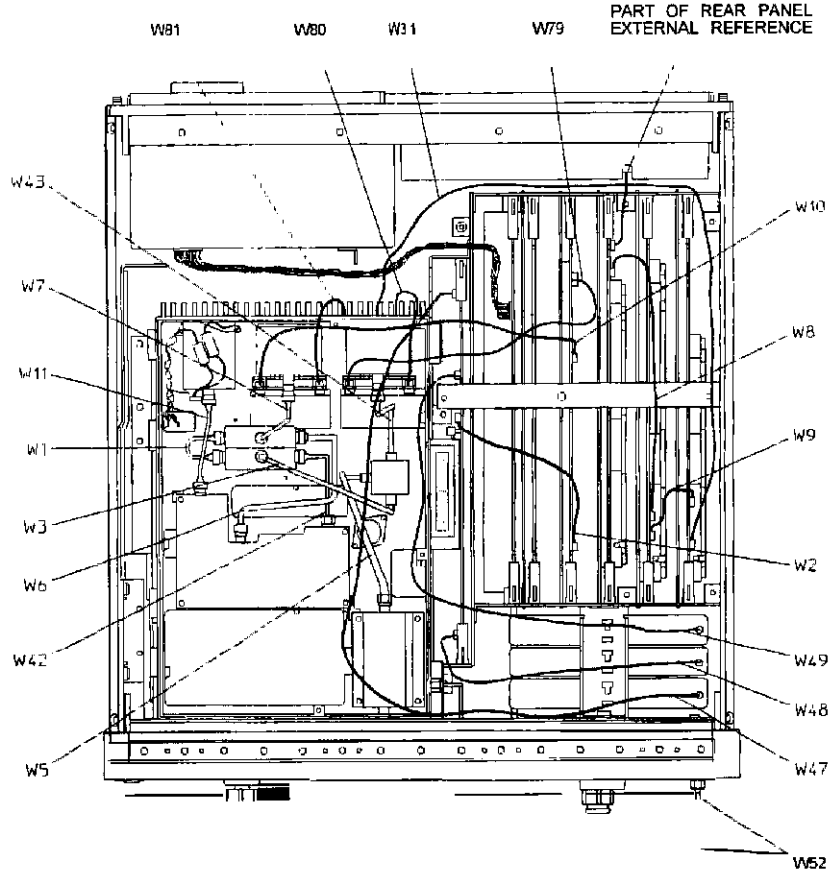
Cables, Top

Ref Desig	Type*	Opt	HP Part Number	Qty	Description
A15W1	18W		(part of A15)	1	A15 to A8 and A17
W1	SR		08720-20064	1	S2 TO A68 (8719D/8720D)
W1	SR		08720-20014	1	S2 TO S3 (8722D)
W2	F		08720-60141	1	A9J3 TO A11J1
W3	SR		08720-20062	1	A58 TO S2 (8719D/8720D)
W3	SR		0-8720-20016	1	S2 TO S1 (8722D)
W5	SR		08722-20017	1	S1 TO A58 (8722D)
W6	SR		08720-20068	1	A63 TO S3
W7	SR		08720-20063	1	A55 TO S3
W8	F		08416-60040	1	A12 TO A13
W9	F		08415-60041	1	A14 TO A13
W10	F		08415-60031	1	A55 TO A11
W11	SR		08720-20065	1	A57 TO A63
W31	F		08415-60035	1	A52 TO A14
W42	SR		08720-20061	1	A63 TO S2
W43	SR		08722-20016	1	A54 TO S1 (8722D)
W47	F		08720-60132	1	A9J1 TO A4
W48	F		08720-60134	1	A9J2 TO A6
W49	F		08720-60133	1	A9J5 TO A5
W79	F		08514-60033	1	A11J3 TO A54J2 (8722D)
W80	F		08720-60131	1	A17J15 TO A64 (8722D)
W81	F		08720-60144	1	A17J15 TO A55

*nW Wire Bundle (n is the number of wires in the bundle)
F Flexible Coax Cable
SR Semi-Rigid Coax Cable


A15W1
W31
PART OF REAR PANEL
EXTERNAL REFERENCE
W31
W10
W7
W8
W11
W9
W1
W2
W3
W49
W6
W48
W42
W47
W17

sb674d


W81
W80
W31
W79
PART OF REAR PANEL
EXTERNAL REFERENCE
W43
W7
W11
W1
W3
W6
W42
W5
W10
W8
W9
W2
W49
W48
W47
W52

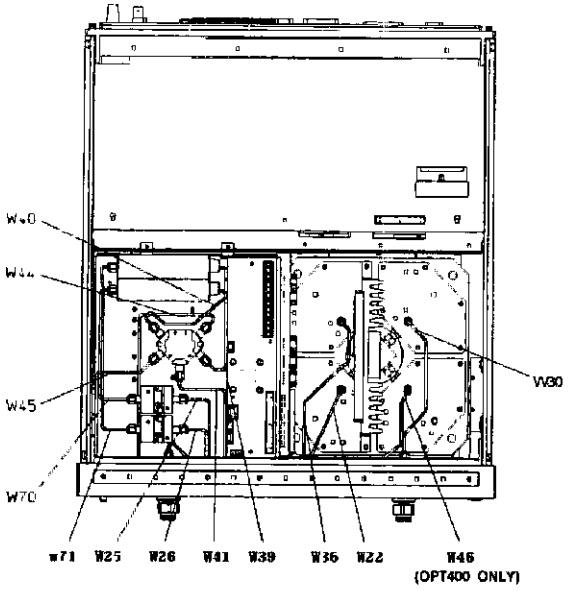
sb6111d

Cables, Bottom

Ref Desig	Type*	Opt	HP Part Number	Qty	Description
W17	SR	085,089	08720-20150	1	S5 TO FRONT PANEL R CHANNEL IN (8719D/8720D)
W17	SR	085,089	08722-20058	1	S5 TO FRONT PANEL R CHANNEL IN (8722D)
W19	SR	086,089	08722-20068	1	S5 TO A58 (8722D)
W19	SR	400	08720-20174	1	A74 TO A56 (8719D/20D)
W19	SR	400	08722-20064	1	A74 TO A55 8722D)
W20	SR	089	08720-20134	1	S5 TO A74
W20	SR	086	08720-20147	1	S5 TO A74
W20	SR	400	08720 20134	1	A76 TO A65 (8719D/20D)
W20	SR	400	08722-20134	1	A76 TO A66 (8722D)
W22	SR		08720 20026	1	A63 TO A66
W24	SR	007	08722-20076	1	S4 TO A69 (8722D)
W25	SR		08720-20249	1	A60 TO A62 (8719D/8720D)
W25	SR		08722-20056	1	A60 TO A62 (8722D)
W26	SR		08720-20025	1	A61 TO A63 (8719D/8720D)
W26	SR		08722 20067	1	A61 TO A63 (8722D)
W27	SR		08720-20248	1	S4 TO A60 (8719D/8720D)
W27	SR		08722 20073	1	S4 TO A60 (8722D)
W27	SR	007	08722-20077	1	S4 TO A60 (8722D)
W28	SR		08720-20011	1	S4 TO A61 (8719D/8720D)
W28	SR		08722-20074	1	S4 TO A61 (8722D)
W28	SR	007	08722-20078	1	S4 TO A61 (8722D)
W29	SR		08720-20009	1	S4 TO A69 (8719D/8720D)
W29	SR		08722-20072	1	94 TO A69 (8722D)
W29	SR	007	08722-20076	1	34 TO A69 (8722D)
W30	SR		08720-20033	1	A62 TO A66
W32	SR	STD,012,			
		007,089	08720-20021	1	A68 TO A69 (8719D/8720D)
W32	SR	086,089	08720-20146	1	A68 TO A69 (8719D/8720D)
W32	SR	STD,012,			
		007,089	08722-20069	1	A68 TO A69 (8722D)
W32	SR	085	08722 20086	1	A68 TO A69 (8722D)
W32	SR	400	08720-20073	1	A68 TO A74 (8719D/8720D)
W32	SR	400	08722-20064	1	A68 TO A74 (8722D)

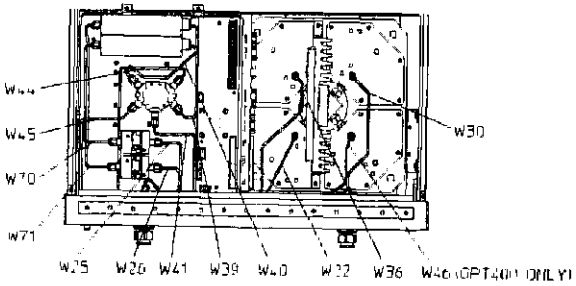
Ref Desig	Type*	Opt	HP Part Number	Qty	Description
W36	SR		08720-20041	1	A72 TO A64
W39	SR		08720-20169	1	A74 TO A70 (8719D/8720D)
W39	SR		08722-20063	1	A74 TO A70 (8722D)
W40	SR		08720-20168	1	A74 TO A71 (8719D/8720D)
W40	SR		08722-20062	1	A74 TO A71 (8722D)
W41	SR		08720-20173	1	A74 TO A58 (8719D/8720D)
W41	SR		08722-20054	1	A74 TO A58 (8722D)
W44	SR	400	08720-20171	1	A74 TO A76 (8719D/8720D)
W44	SR	400	08722-20055	1	A74 TO A76 (8722D)
W45	SR		08720-20174	1	A74 TO S5 (8719D/8720D)
W45	SR		08722-20064	1	A74 TO S5 (8722D)
W46	SR		08720-20103	1	A67 TO A73
W52	SR	STD, 012, 085	08720-20075	1	JUMPER (8719D/8720D)
W52	SR		08722-20024	1	JUMPER (8722D)
W58	SR	085	08720-20135	1	A69 TO REAR PANEL SOURCE OUT (8719D/8720D)
W58	SR	085	08722-20085	1	A69 TO REAR PANEL SOURCE OUT (8722D)
W59	SR	085	08720-20144	1	S4 TO REAR PANEL SOURCE IN (8719D/8720D)
W59	SR	085	08722-20084	1	S4 TO REAR PANEL SOURCE IN (8722D)
W60	SR	085	08720-20159	1	S4 TO PORT 2 SWITCH (8719D/8720D)
W60	SR	085	08722-20097	1	S4 TO PORT 2 SWITCH (8722D)
W64	SR	085	08720-20143	1	A62 TO A70
W65	SR	085	08720-20168	1	A66 TO A70
W66	SR	085	08720-20157	1	A66 TO A71
W67	SR	085	08720-20142	1	A63 TO A71
W70	SR	400	08720-20145	1	A60 TO A75 (8719D/8720D)
W70	SR	400	08722-20061	1	A60 TO A76 (8722D)
W71	SR	400	08720-20136	1	A61 TO A76 (8719D/8720D)
W71	SR	400	08722-20059	1	A61 TO A76 (8722D)

* SR Semi-Rigid Coax Cable

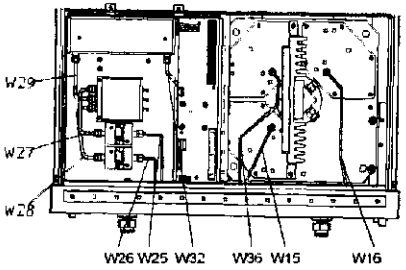


HP 8719D/20D/22D OPTION 400

sb6136d

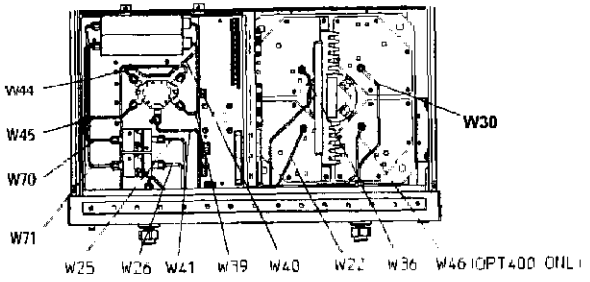


HP 8719D/20D/22D OPTION 400

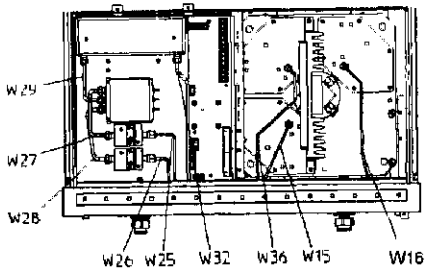


HP 8719D/20D/22D OPTION 012

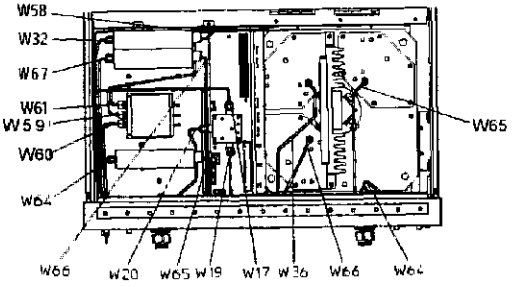
sb6 B3d



HP 8719D/20D/22D OPTIONS 400

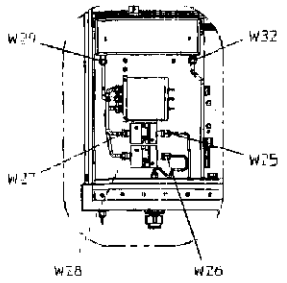


HP 8719D/20D/22D OPTIONS 012

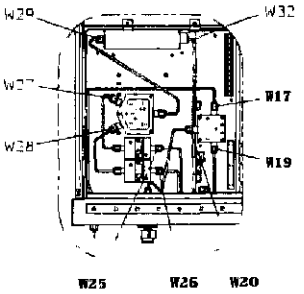


HP 8719D/20D/22D OPTIONS 085,089

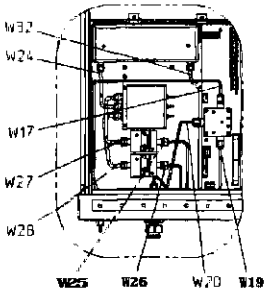
sb6137d



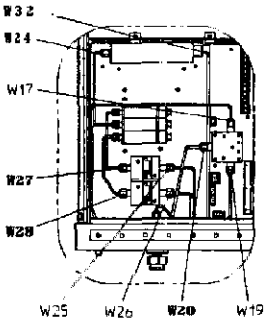
HP 8719D/20D
STANDARD



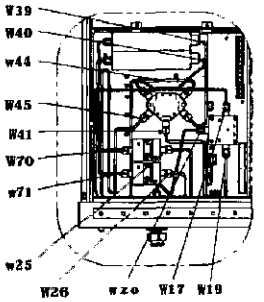
HP 87220
OPTION 089



HP 8719D/20D
OPTION 089



HP 8719D/20D/22D
OPTIONS 007,089



HP 8719D/20D/22D
OPTIONS 400,089

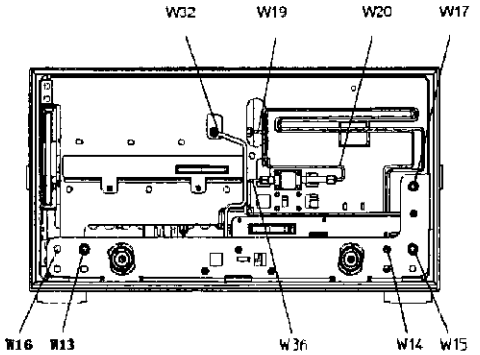
sb6138d

Cables, Front

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
A19			08720-60130	1	SD ASSY-GSP
A22			08720-60152	1	BD ASSY-DISPLAY INTERFACE (NOT SHOWN)
A56			08720-60182	1	SD ASSY-LED
A72,A73			5086-7649	2	R CHANNEL BUFFER AMPLIFIER
A75,A76			8490D OPT 006	2	ATTENUATOR 6 DB
A75,A76		400	8490D OPT 010	2	ATTENUATOR 10 DB (8722D)
W13	SR	012	08720-20164	1	A62 TO FRONT PANEL OUT (8719D/8720D)
W14	SR	012	08720-20154	1	A63 TO FRONT PANEL OUT (8719D/8720D)
W13,W14	SR	012	08722-20102	1	A62 A63 TO FRONT PANEL OUT (8722D)
W15	SR	012	08720-20058	1	A66 TO FRONT PANEL IN (8719D/8720D)
W15	SR	012	08722-20079	1	A66 TO FRONT PANEL IN (8722D)
W16	SR	012	08720-20104	1	A66 TO FRONT PANEL IN (8719D/8720D)
W16	SR	012	08722-20081	1	A65 TO FRONT PANEL IN (8722D)
W17	SR	085,089	08720-20105	1	S5 TO FRONT PANEL R CHANNEL IN (8719D/8720D)
W17	SR	085,089	08722-20068	1	S5 TO FRONT PANEL R CHANNEL IN (8722D)
W19	SR	085,089	08722-20058	1	S5 TO A68 (8722D)
W20	SR	089	08720-20134	1	36 TO A76
W20	SR	085	08720-20147	1	S5 TO A76
W23	SR		08720-20047	1	A68 TO FRONT PANEL R CHANNEL OUT (8719D/20D)
W23	SR		08722-20071	1	A68 TO FRONT PANEL R CHANNEL OUT (8722D)
W32	SR	STD,012,			
		007,089	08720-20021	1	A68 TO A69 (8719D/8720D)
W32	SR	086,089	08720-20146	1	A68 TO A69 (8719D/8720D)
W32	SR	STD,012,			
		007,089	08722-20069	1	A68 TO A69 (8722D)
W32	SR	086	08722-20086	1	A68 TO A69 (8722D)
W33	SR		08720-20046	1	A76 TO FRONT PANEL R CHANNEL IN (8719D/20D)
W33	SR		08722-20098	1	A76 TO FRONT PANEL R CHANNEL IN (8722D)
W36	SR		08720-20041	1	A76 TO A64
W41	SR	400	08720-20173	1	A74 TO A68 (8719D/8720D)
W41	SR	400	08722-20054	1	A74 TO A68 (8722D)
W60	SR	086	08720-20159	1	S4 TO PORT 2 SWITCH (8719D/8720D)
W60	SR	086	08722-20097	1	S4 TO PORT 2 SWITCH (8722D)
W61	SR	086	08720-20161	1	S4 TO PORT 1 SWITCH (8719D/8720D)
W61	SR	085	08722-20098	1	S4 TO PORT 1 SWITCH (8722D)

Ref. Desig.	Type*	Opt	HP Part Number	Qty	Description
W62	SR	085	08720-20162	1	A63 TO PORT 2 COUPLER (8719D/8720D)
W62	SR	085	08720-20103	1	A63 TO PORT 2 COUPLER (8722D)
W63	SR	085	08720-20163	1	A62 TO PORT 1 COUPLER (8719D/8720D)
W63	SR	085	08722-20104	1	A62 TO PORT 1 COUPLER (8722D)
W68	SR	012,086			
		089	08720-20165	1	A71 TO FRONT PANEL B IN (8719D/8720D)
W68	SR	012,085,			
		089	08722-20099	1	A71 TO FRONT PANEL B IN (8722D)
W69	SR	012,085			
		089	08720-20166	1	A70 TO FRONT PANEL A IN (8719D/8720D)
W69	SR	012,085,			
		089	08722-20101	1	A70 TO FRONT PANEL A IN (8722D)
W73	SR	400	08720-20169	1	A74 TO A76
W75	SR	400	08720-20171	1	A74 TO A76 (8719D/8720D)
W75	SR	400	08722-20055	1	A74 TO A75 (8722D)
W77	SR	400	08720-20103	1	A67 TO A76

*SR Semi-Rigid Coax Cable



HP 8719D/20D/22D OPTIONS 007,012,089

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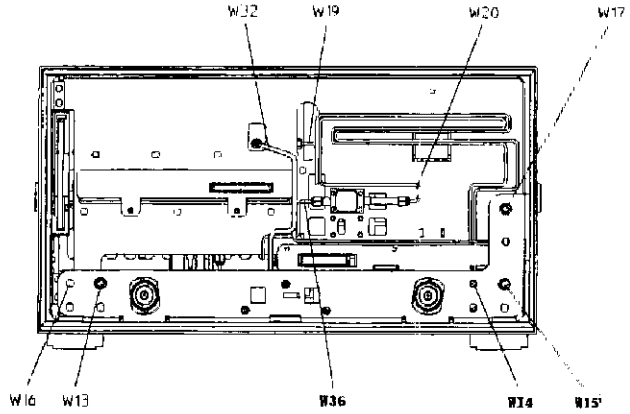
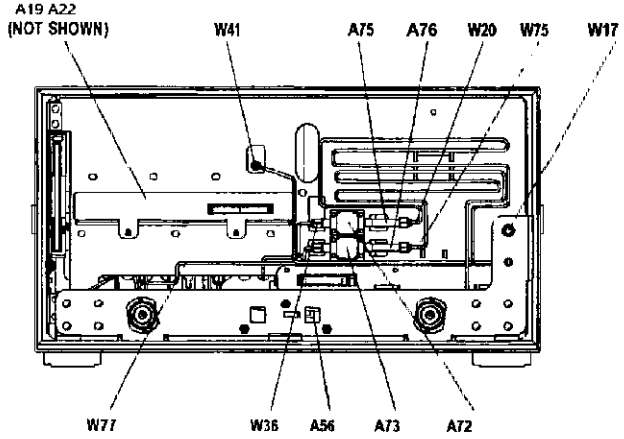
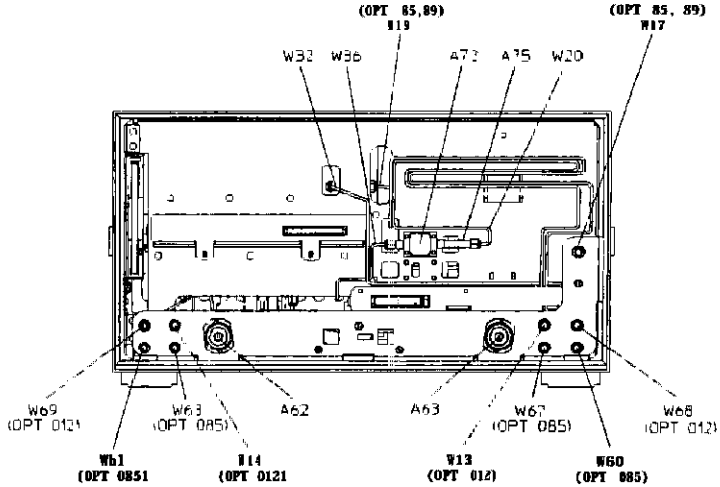


HP 8719D/20D/22D OPTIONS 007,012,089

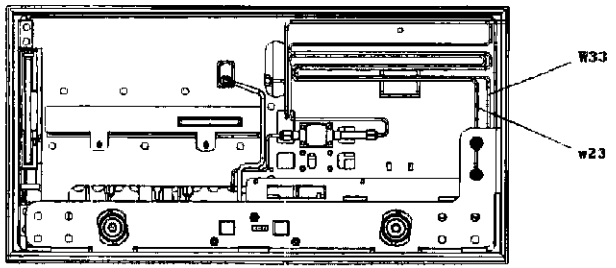


HP 8719D/20D/22D OPTIONS 400,089

sb61f4d



HP 8719D/20D/22D OPTION 085,012,089



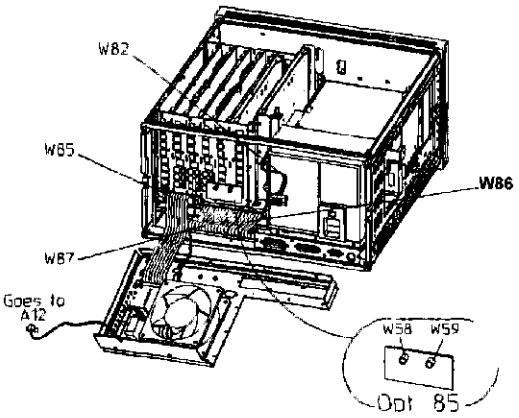
HP 8719D/20D STANDARD

sb6112d

Cables, Rear

Ref Desig.	Type*	Opt	HP Part Number	Qty	Description
W52	SR	086	08720-20098	1	REAR PANEL SOURCE OUT TO IN (W58 TO W59) (8719D/20D
W52	SR	085	08722-20024	1	REAR PANEL SOURCE OUT TO IN (W58 TO W59 (8722D)
W58	SR	085	08720-20135	1	A69 TO REAR PANEL SOURCE OUT (8719D/8720D)
W58	SR	085	08722-20085	1	A69 TO REAR PANEL SOURCE OUT (8722D)
W59	SR	085	08720-20144	1	S4 TO REAR PANEL SOURCE IN (8719D/8720D)
W59	SR	085	08722-20084	1	S4 TO REAR PANEL SOURCE IN (8722D)
W82	1W		8120-6876	1	VGA OUT TO A2252
W85	3W		8120-6407	1	A16 TO A17
W86	2W		8120-6382	1	A7 TO A17
W87	5W		8120-6379	1	A7 TO A17

*nW Wire Bundle (n is the number of wires in the bundle)



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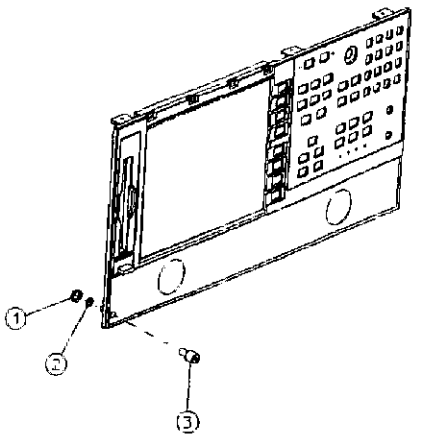
Front Panel Assembly, Outside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		2950-0006	1	NUT HEX 1/4 32
2		2190-0067	1	WASHER LK 256 ID
3		1510-0038	1	GROUND POST



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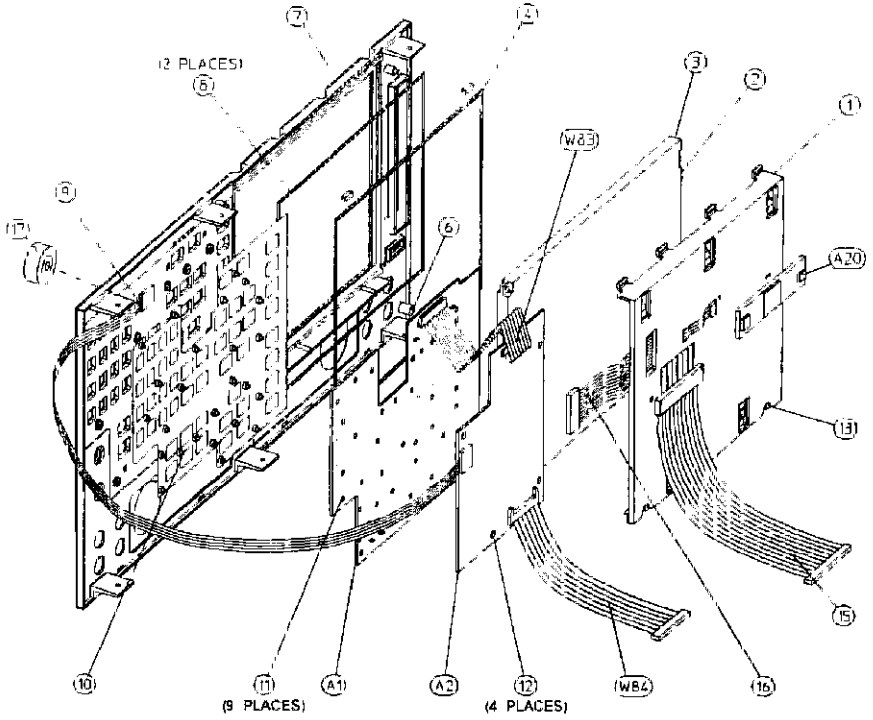
Front Panel Assembly, Inside

Ref. Desig	Option	HP Part Number	Qty	Description
1		08720-40012	1	DISPLAY HOLD DOWN
2		2090-0566	1	DISPLAY LAMP
3		08720-60160	1	ASSY-COLOR LCD (A18)
4		1000-0995	1	DISPLAY GLASS
6		2190-0067	1	WASHER LK 256 ID
6		2950-0006	1	NUT HEX 1/4-32
7	STD 089	08720-60162	1	**FRONT PANEL ASSY**
7	012	08720-60163	1	FRONT PANEL ASSY
7	085	08720-60164	1	FRONT PANEL -ASSY
7	012 085	08720-60165	1	FRONT PANEL ASSY
8		08720-00096	2	GASKET
9		1990-1864	1	RPG (INCLUDES CABLE AND HARDWARE)
10		08720-40010	1	FLUBBER KEYPAD
11		0615-0430	9	SCREW SM 3 0 6 CWPNTX
12		0515-0665	4	SCREW SMM 3 0 14 CWPNTX
13		0515-0372	3	SCREW SMM 3 0 8 CWPNTX
16		8120-6892	1	CABLE-GSP TO FLEX CIRCUIT
16		08720-60180	1	CABLE-FLEX CIRCUIT
17		E4400-40003	1	RPG KNOB
18		08719-80022	1	8719D NAME PLATE (not shown)
18		08720-80045	1	8720D NAME PLATE (not shown)
18		08722-80019	1	8722D NAME PLATE (not shown)
A1		08720-60127	1	BD ASSY-FRONT PANEL
A2		08720-60128	1	BD ASSY-FRONT PANEL INTERFACE
A20		0960-3068	1	ASSY-INVERTER
W83		8120-6432	1	A1 TO A2
W84		08720-60074	1	A2 TO A17



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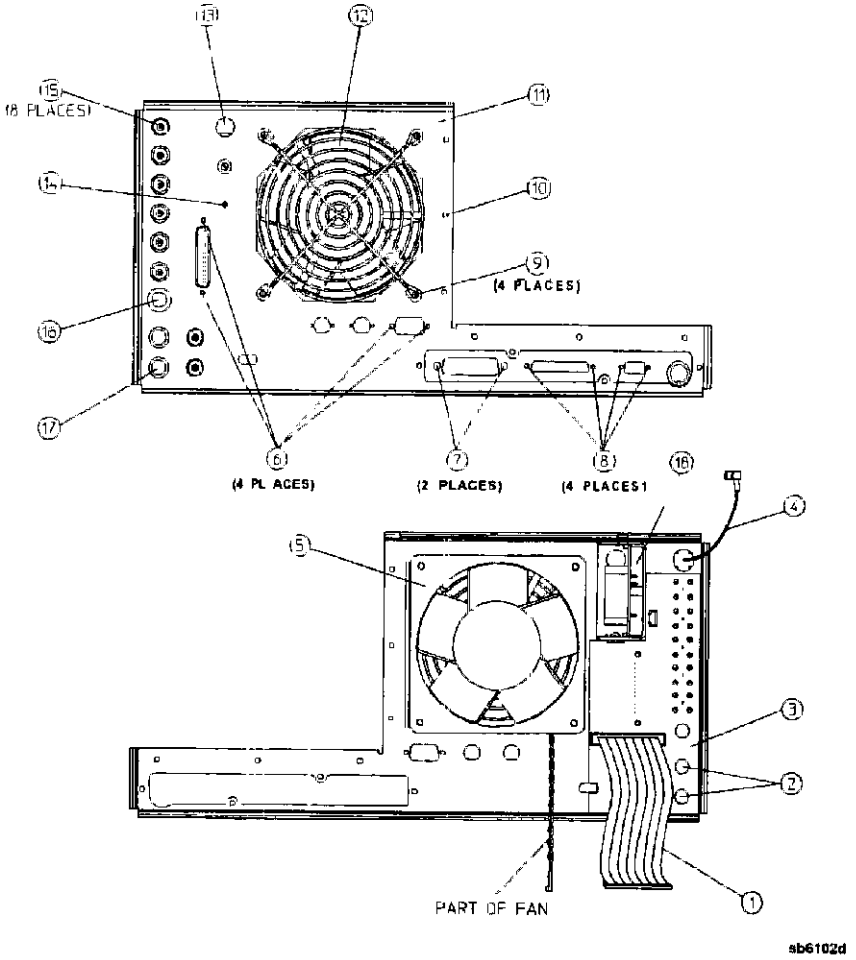
Rear Panel Assembly

Ref Desig	Option	HP Part Number	Qty	Description
1		8120-6407	1	W85-A17 TO A16
2		85049-60005	2	ASSY-FUSE
3		08720-60138	1	BD ASSY-REAR PANEL INTERFACE (A16)
4		08753-60026	1	ASSY-EXTERNAL REFERENCE CABLE
5		08415-60036	1	ASSY-FAN
6		1251-2942	4	FASTENER CONN RP LOCK
7		2190-0034	2	WASHER LK .194ID10
7		0380-0644	2	NUT STDF 327L 6-32
8		1251-2942	4	FASTENER CONN RP LOCK
9		0515-2040	4	SCREW SMM 3.6 16 PCFLTX
10		0615-0372	10	SCREW SMM 3.0 8 CWPNTX
11		08720-00071	1	REAR PANEL
12		3160-0281	1	FAN GUARD
13	1D5	0590-1310	1	NUT SPCL 1/2-28
13	1D5	2190-0068	1	WASHER LK .505ID
14	1D5	0515-0372	1	SCREW SMM 3.0 8 CWPNTX
15		2190-0102	1	WASHER LK .472ID
15		2950-0035	8	NUT HEX 15/32-32
16		0400-0271	8	GROMMET SN 5-515ID
17		2110-0047	2	FUSE
17		1400-0112	2	FUSE CAP
18	1D5			(see "Rear Panel Assembly, Option 1D5")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(4 PLACES)
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(4 PLACES)
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(2 PLACES)
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(4 PLACES)
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PART OF FAN
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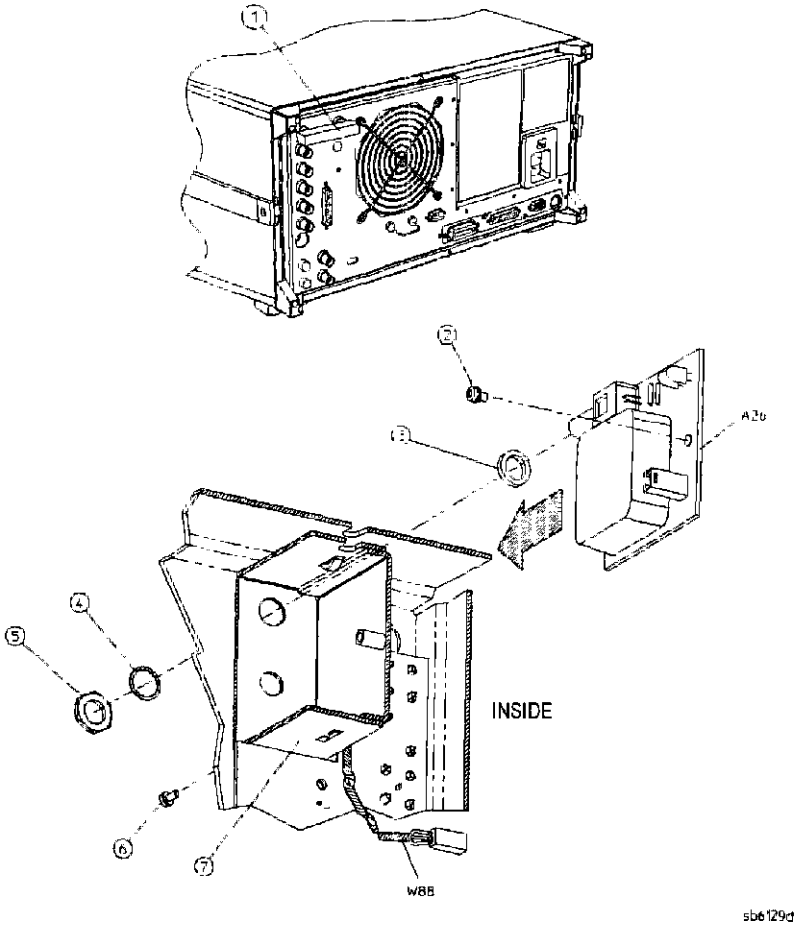
Rear Panel Assembly, Option 1D5

Ref. Desig.	Option	HP Part Number	Qty	Description
1	1D5	1250-1859	1	ADAPTER-COAX
2	1D5	0515-0374	1	SCREW-MACHINE M3 0X 10 CW-PN-TX
3	1D5	3050-1546	1	WASHER FLAT 505ID NY
4	1D5	2190-0068	1	WASHER LOCK 505ID
5	1D5	0590-1310	1	NUT-SPECIALTY 1/2-28
6	1D5	0515-0430	1	SCREW-MACHINE M3 0x6 CW-PN-TX
7	1D5	08753-00078	1	BRACKET-OSC BD
A26	1D5	08753-60158	1	BD ASSY-HIGH STABILITY FREQ REF
W88	1D5	8120-6458	1	RP INTERFACE (A16J3) to HIGH-STABILITY FREQ REF (A26J1)


1
2
A26
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INSIDE
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7
W88
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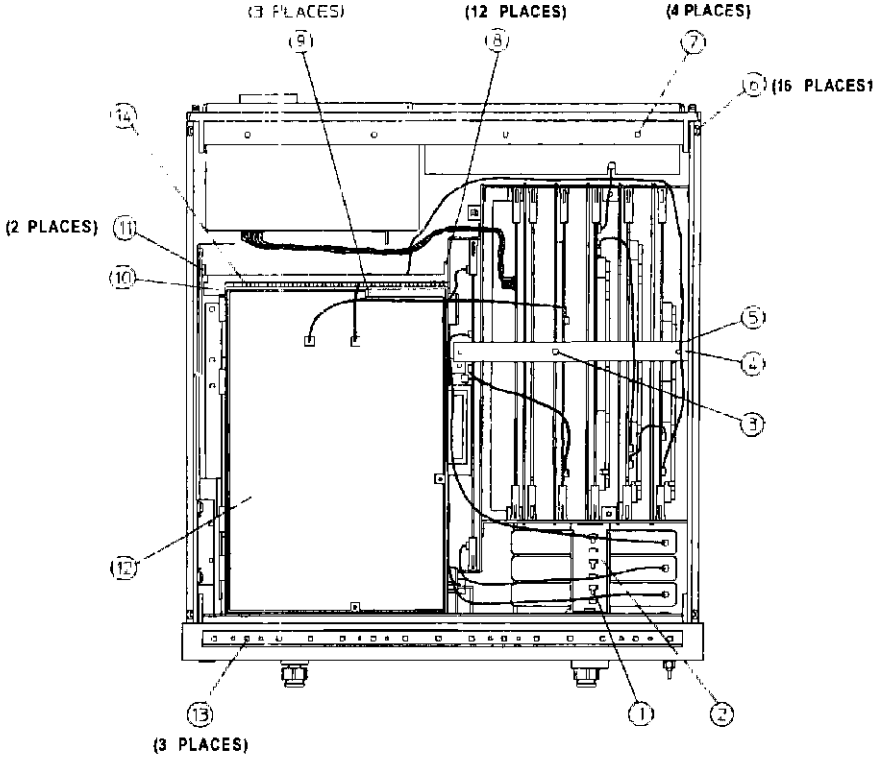
Hardware, Top

Ref. Desig	Option	HP Part Number	Qty	Description
1		08720-40004	3	LOCATOR HOLD DOWNS
2		08720-00066	1	CAN HOLD DOWN
3		0515-2035	1	SCREW SMM 3.0 16 PCFLTX
4		08753-20062	1	PC STABILIZER CAP
5		08720-40001	1	PC BOARD STABILIZER
6		0615-2086	16	SCREW SMM 4.0 7 PCFLTX
7		0515-0458	4	SCREW SMM 3.6 10 CWPNTX
8		0515-0431	2	SCREW SMM 3.5 6 CWPNTX
9		0515-430	3	SCREW SMM 3.0 6 CWPNTX
10		08720-00023	1	SOURCE HOLD DOWN
11		0515-0377	2	SCREW SMM 3.5 10 CWPNTX
12		08720-00038	1	SOURCE COVER
13		0615-1400	3	SCREW SMM 3.6 8 PCFLTX
14		08720-20185	1	SOURCE CASTING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(12 PLACES)
(4 PLACES)
(16 PLACES)
(2 PLACES)
(3 PLACES)
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13
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2

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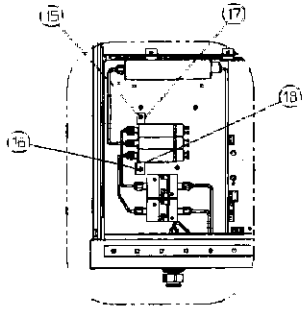
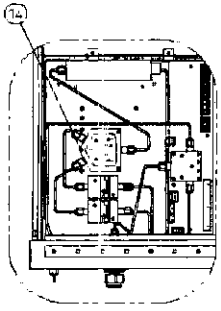
Hardware, Bottom

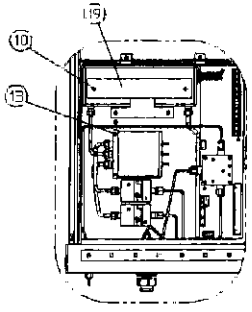
Ref. Desig	Option	HP Part Number	Qty	Description
1		0515 0430	1	SCREW SMM 3.0 6 CWPNTX
2		0515-0458	4	SCREW SMM 3 6 8 CWPNTX
3		0515-0430	2	SCREW SMM 3.0 6 PCFLTX
4		0515-2086	6	SCREW SMM 4.0 7 PCFLTX
5		0516-1400	4	SCREW SMM 3 5 8 PCFLTX
6		0515-0433	4	SCREW SMM 4.0 S CWPNTX
6		3050-0001	4	WASHER FL 1721
7		0515-0375	4	SCREW SMM 3.0 6 CWPNTX
8		0515-0430	4	SCREW SMM 3.0 6 CWPNTX
9		0615 1400	1	SCREW SMM 3 5 8 PCFLTX
10		2200-0105	2	SCREW SM 440 312 PCFLTX
11		0515-0375	4	SCREW SMM 3.0 16 CWPNTX
12		0515-0375	2	SCREW SMM 3.0 16 CWPNTX
13		0515-0666	2	SCREW SMM 3.0 18 CWPNTX
14		0515-0665	3	SCREW SMM 3.0 14 CWPNTX
15		0515-0430	2	SCREW SMM 3.0 6 CWPNTX
16		08722-00016	2	SWITCH BRACKET
17		0515-2194	1	SCREW SMM 3.0 50 CWPNTX
18		0636 0031	1	NUT HEX SMM 3.0
19		08720-00113	1	BRACKET, ATTENUATOR



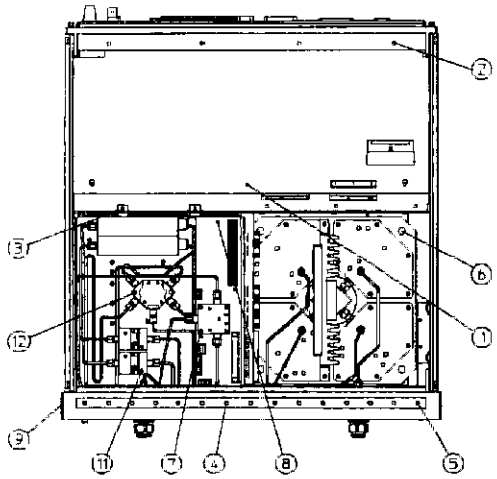
HP 8722D
OPTION 007



HP 8722D



HP 8719D/20D



HP 8722D
OPTION 400

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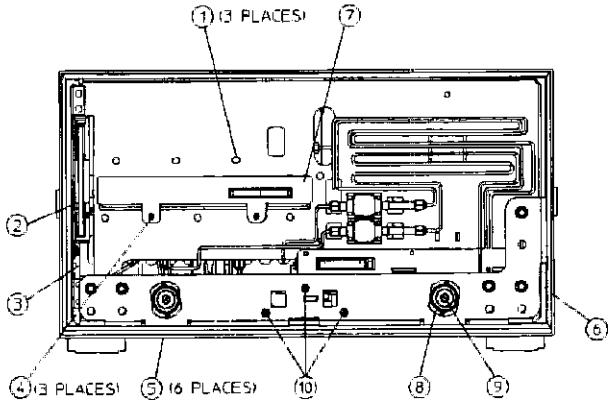
Hardware, Front

Ref. Desig.	Option	HP Part Number	Qty	Description
1		**0615 0382**	3	SCREW SMM 4.0 12 CWINTX
2		08720-00021	1	DISK DRIVE BRACKET
2		0505-1934	4	SCREW SMM 2.5 6 CWPNTX
3		08720-00077	1	ACTUATOR SWITCH ARM
3		08720-40014	1	AC LINE BUTTON
4		0515 0430	2	SCREW SMM 3.0 6 CWPNTX
5		0515-2086	6	SCREW SMM 4.0 7 PCFLTX
6		0515-1400	1	SCREW SMM 3.5 8 PCFLTX
7		08720-00093	1	CABLE MOUNTING BRACKET
8		5022-1087	2	NUT-FLANGE
9		08720-60159	1	TEST PORT CONNECTOR REPLACEMENT KIT (HP 8719D/20D)
9		08517-60027	1	TEST PORT CONNECTOR REPLACEMENT KIT (HP 8722D)
10		0515 0430	3	SCREW SMM 3.0 6



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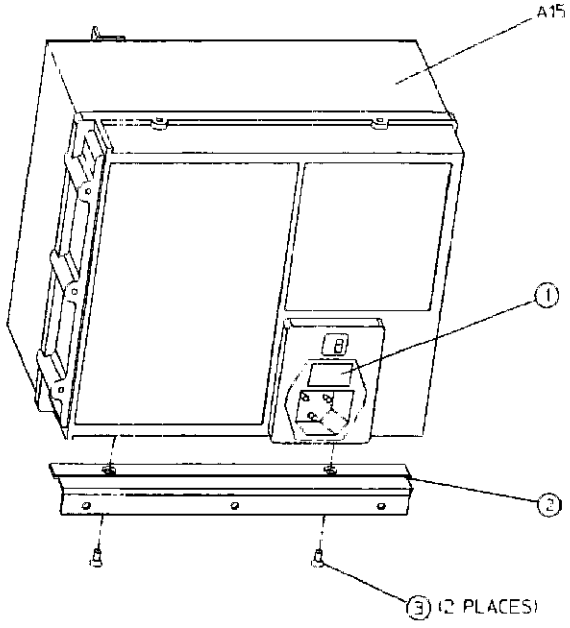
Hardware, Preregulator

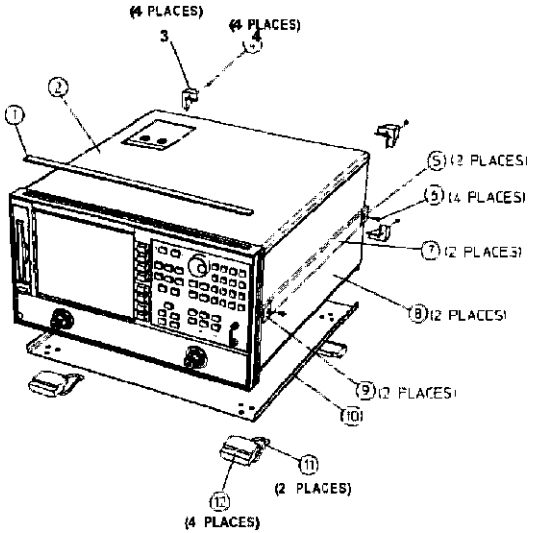
Ref. Desig.	Option	HP Part Number	Qty	Description
1		2110-0780	1	FUSE 3A 250 V NON-TIME DELAY
2		08753-00065	1	BRACKET-PREREGULATOR
3		0515-1400	2	SCREW-MACHINE M3.5x8 CW-FL-TX
A15		08753-60098	1	PREREGULATOR-ASSY
A15		08753-69098	1	PREREGULATOR-ASSY (REBUILT-EXCHANGE)



sg691d

Chassis Parts, Outside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		5041-9176	2	TRIM STRIP
2		08720-00078	1	COVER-TOP
3		5041-9188	4	REAR STANDOFF
4		0516-1402	4	SCREW SMM 3 6 8 PCPNTX
5		5041-9187	2	REAR CAP-SIDE STRAP
6		0515-1384	4	SCREW SMM 6 0 10 PCFLTX
7		08720-00081	2	SIDE STRAP
8		08720-00080	2	COVER-SIDE
9		5041-9186	2	FRONT CAP-SIDE STRAP
10		08720-00079	2	COVER-BOTTOM
11		1460-1345	2	FOOT ELEVATOR
12		5041-9167	4	FOOT



Chassis Parts, Inside

Ref. Desig.	Option	HP Part Number	Qty	Description
1		5022-1190	1	FRONT PANEL FRAME
2		0515-0375	1	SCREW 5MM 3 0 16 CWPNTX
3		08720-00076	1	MEMORY DECK
4		0515-0458	4	SCREW SMM 3 5 8 CWPNTX
5		5021-5808	1	REAR FRAME
6		0515-2086	16	SCREW SMM 4 0 7 PCFLTX
7		08720-20131	4	SIDE STRUTS
8		08720-60116	1	ASSY-CHASSIS
9			1	ASSY-DISK DRIVE
A17		08720-60170	1	BD ASSY-MOTHERBOARD

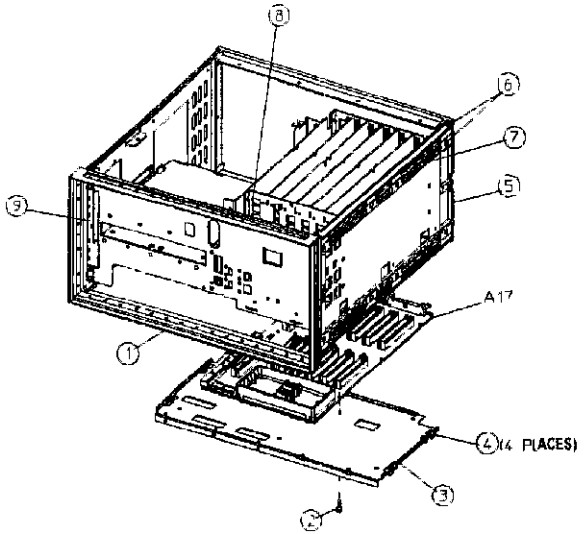


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Table 13-1. Miscellaneous Replaceable Parts

Description	HP Part Number
Service Tools	
HP 8719D/8720D/8722D TOOL KIT *includes the following*	08722-60018
ADAPTER 2.4-mm (F) APC 3.5 (F)	
ADAPTER 2.4-mm (F) APC 3.5 (M)	
EXTENDER BOARD ASSEMBLY-FOR 2ND CONVERTERS	
EXTENDER BOARD ASSEMBLY	
SOURCE CONTROL EXTENDER BOARD ASSEMBLY	
ADAPTER SMB (M) TO SMB (M)	
ADAPTER SMB (F) TO BNC (F)	
ADAPTER-SMA (F) TO SMA (F)	
ADAPTER SMA (M) TO SMA (M)	
SMB TEE	
FUSE .5A 125 V	
FUSE 1A 125 V	
FUSE 2A 125 V	
FUSE 4A 125 V	
FUSE 3.15A 250 V	
CABLE ASSEMBLY-EXTENDER RF	
CABLE ASSEMBLY-SMA FLEX	
WRENCH-OPEN ENDED 6.5	
BAG-ANTISTATIC 12.0 X 15.0D	
Documentation	
HP 8719D/8720D/8722D SERVICE GUIDE	08720-90292
HP 8719D/8720D/8722D MANUAL SET *includes the following*	08720-90282
HP 8753D EXAMPLE PROGRAM DISK #1 HP BASIC	0876310028
HP 8753D EXAMPLE PROGRAM DISK #2 QUICKC AND QUICK BASIC	0876310029
HP 8719D/8720D/8722D PROGRAMMERS GUIDE	08720-90293
HP 8719D/8720D/8722D USER'S GUIDE *(includes Quick Reference, 08720-90286)*	08720-90288
HP 8719D/8720D/8722D INSTALLATION/QUICK START GUIDE	08720-90291

Table 13-1. Miscellaneous Replaceable Parts (continued)

Description	HP Part Number
Upgrade Kits	
FIRMWARE UPGRADE KIT	08720-60168
MECHANICAL TRANSFER SWITCH UPGRADE KIT[1]	OPTION 007
TIME DOMAIN CAPABILITY UPGRADE KIT[1]	OPTION 010
DIRECT SAMPLER ACCESS UPGRADE KIT[1]	OPTION 012
HIGH-POWER S-PARAMETER TEST SET UPGRADE KIT[1]	OPTION 085
FREQUENCY OFFSET MODE UPGRADE KIT[1]	OPTION 089
HIGH-STABILITY FREQUENCY REFERENCE UPGRADE KIT[1]	OPTION 1D5
FOURTH SAMPLER AND TRL CALIBRATION FIRMWARE UPGRADE KIT[1]	OPTION 400
Protective Caps for Connectors	
FEMALE HP-IB CONNECTOR	1252-5007
FEMALE PARALLEL PORT	1252-4690
RS-232 CONNECTOR	1252-4697
7-mm TEST PORTS	1401-0249
FEMALE 3.5 MM TEST PORTS	1401-0245
Fuses used on the A8 Post Regulator	
FUSE 2A 125 V NON-TIME DELAY 0.25x0.27	2110-0425
FUSE 0.75A 126 V NON-TIME DELAY 0.25x0.27	2110-0424
FUSE 2A 125 V NON-TIME DELAY 0.26x0.27	2110-0426
FUSE 4A 126 V NON-TIME DELAY 0.25x0.27	2110-0476
FUSE 1A 125 V NON-TIME DELAY 0.26x0.27	2110-0047
FUSE 0.5A 126 V NON-TIME DELAY 0.25x0.27	2110-0046
HP-IB Cables	
HP-IB CABLE, 1M (3.3 FT)	HP 10833A
HP-IB CABLE, 2M (6.6 FT)	HP 10833B
HP-IB CABLE, 4M (13.2 FT)	HP 10833D
HP-IB CABLE, 0.5M (1.6 FT)	HP 10833D
Touch-up Paint	
DOVE GRAY *for use on frame around front panel and painted portion of handles*	6010-1146
FRENCH GRAY *for use on side, top, and bottom covers*	6010-1147
PARCHMENT WHITE *for use on rack mount flanges, rack support flanges, and front panels*	6010-1148

Order the model number (HP 8719DU, 8720DU, 8722DU) plus the upgrade option designation

Table 13-1. Miscellaneous Replaceable Parts (continued)

Description	HP Part Number
ESD Supplies	
ADJUSTABLE ANTISTATIC WRIST STRAP	9300-1367
5 FT GROUNDING CORD *for wrist strap*	9300-0980
2 X 4 FT ANTISTATIC TABLE MAT WITH 15 FT GROUND WIRE	9300 0797
ANTISTATIC HEEL STRAP *for use on conductive floors*	9300-1126
Other	
KEYBOARD OVERLAY *for external keyboard*	08753-80111
SYSTEM RACK KIT, ALSO ORDER THE FOLLOWING:	HP 85043D
FILLER PANEL-7 INCH	HP 40104A
RACK MOUNT FLANGE KIT *for instruments with handles*	5063-9223
RACK MOUNT FLANGE KIT, *includes instrument handles*	5063-9236
RACK MOUNT FLANGE KIT, *instrument handles not included*	5063-9216
FRONT HANDLE	5063-9229
FLOPPY DISKS, 3 5 INCH DOUBLE-SIDED (box of 10)	HP 92192A

Table 13-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS	
A	assembly
B	fan, motor
J	electrical connector (stationary portion) jack
RPG	rotary pulse generator
W	cable, transmission path, wire

ABBREVIATIONS	
A	ampere
ALC	automatic level control
ASSY	assembly
AUX	auxiliary
BD	board
COAX	coaxial
CPU	central processing unit
CW	conical washer (screws)
D	diameter
ESD	electrostatic discharge
EXT	external
EYO	YIG oscillator
FL	flathead (screws)
FP	front panel
FRAC-N	fractional N
FREQ	frequency
GHz	gigahertz
HEX	hexagonal
HP	Hewlett-Packard
HP-IB	Hewlett-Packard interface bus
HX	hex recess (screws)
ID	inside diameter
IF	intermediate frequency
I/O	input/output
LED	light-emitting diode
M	meters
M	metric hardware
MHz	megahertz
mm	millimeters
MON	monitor
NOM	nominal
NY	nylon
OD	outside diameter
Opt	option
OSC	oscillator
PN	panhead
PC	patch lock (screws)
PC	printed circuit
PIG	peripheral interface group
PN	panhead (screws)
REF	reference
REPL	replacement
RP	rear panel
SH	socket head cap (screws)
TX	TORX recess (screws)
Qty	quantity
V	volt
WFR	wire formed
W/O	without
YIG	yttrium-iron garnet

14

Assembly Replacement and Post-Repair Procedures

This chapter contains procedures for removing and replacing the major assemblies of the HP 8719D/8720D/8722D network analyzer. A table showing the corresponding post-repair procedures for each replaced assembly is located at the end of this chapter.

Replacing an Assembly

The following steps show the sequence to replace an assembly in an HP 8719D/8720D/8722D Network Analyzer.

1. Identify the faulty group. Refer to Chapter 4, "Start, Troubleshooting Here." Follow up with the appropriate troubleshooting chapter that identifies the faulty assembly.
2. Order a replacement assembly. Refer to Chapter 13, "Replaceable Parts."
3. Replace the faulty assembly and determine what adjustments are necessary. Refer to Chapter 14, "Assembly Replacement and Post-Repair Procedures."
4. Perform the necessary adjustments. Refer to Chapter 3, "Adjustments and Correction Constants."
5. Perform the necessary performance tests. Refer to Chapter 2, "System Verification and Performance Tests."

Warning **These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.**

Warning **The opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.**

Warning **The power cord is connected to internal capacitors that may remain live for 10 seconds after disconnecting the plug from its power supply.**

Caution Many of the assemblies in this instrument are very susceptible to damage from ESD (electrostatic discharge). Perform the following procedures only at a static-safe workstation and wear a grounding strap.

Procedures Described in this Chapter

The following pages describe assembly replacement procedures for the HP 8719D/8720D/8722D assemblies listed below:

- Line Fuse
- Covers
- Front, Panel Assembly
- Front Panel Interface and Keypad Assemblies
- Display Lamp and Assembly
- Rear Panel Assembly
- Rear Panel Interface Board Assembly
- Source Assemblies
- A7 CPU Board Assembly
- A7BT1 Battery
- AI5 Preregulator Assembly
- A19 Graphics Processor Assembly
- A3 Disk Drive Assembly
- A62, A63 Test Port Couplers and LED Board Assemblies
- A26 High Stability Frequency Reference (Option 1D5) Assembly
- B1 Fan Assembly

Line Fuse

Tools Required

- small slot screwdriver

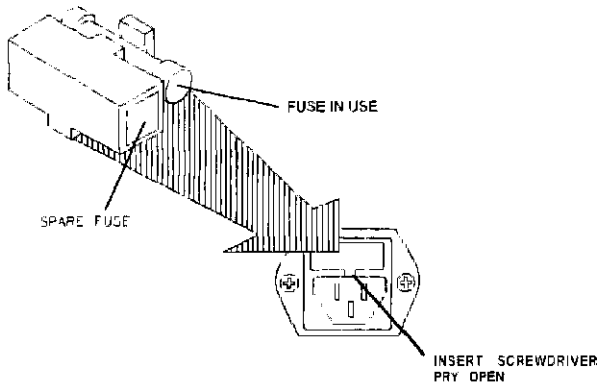
Removal

Warning **For continued protection against fire hazard, replace fuse only with same type and rating (3 A 250 V F). The use of other fuses or materials is prohibited.**

1. Disconnect the power cord.
2. Use a small slot screwdriver to pry open the fuse holder.
3. Replace the blown fuse with a 3 A 250 V F fuse (HP part number 2110-0708).

Replacement

1. Replace the fuse holder.



qq652d

Covers

Tools Required

- T- 10 TORX screwdriver
- T-15 TORX screwdriver
- T-20 TORX screwdriver

Removing the top cover

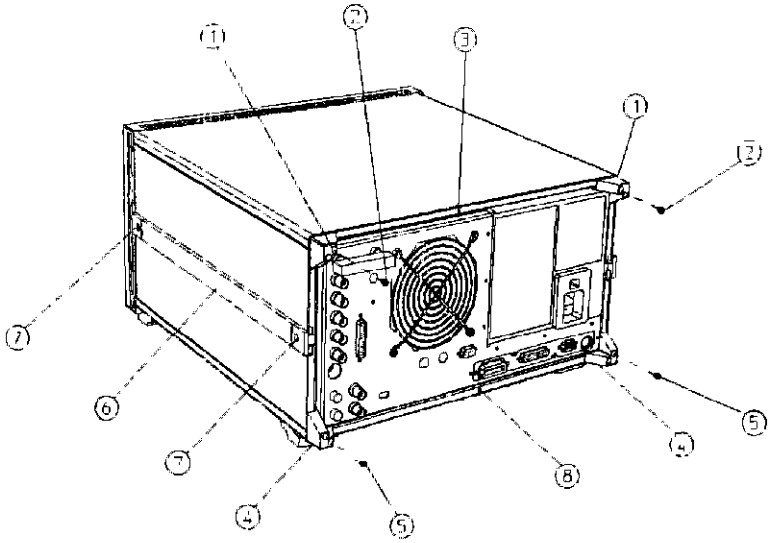
1. Remove both upper rear feet (item 1) by loosening the attaching screws (item 2).
2. Loosen the top cover screw (item 3).
3. Slide cover off.

Removing the side covers

1. Remove the top cover.
2. Remove the lower rear foot (item 4) that corresponds to the side cover you want to remove by loosening the attaching screw (item 5).
3. Remove the handle assembly (item 6) by loosening the attaching screws (item 7).
4 Slide cover off.

Removing the bottom cover

1. Remove both lower rear feet (item 4) by loosening the attaching screws (item 5).
2. Loosen the bottom cover screw (item 8).
3. Slide cover off.



sb686d

Front Panel Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

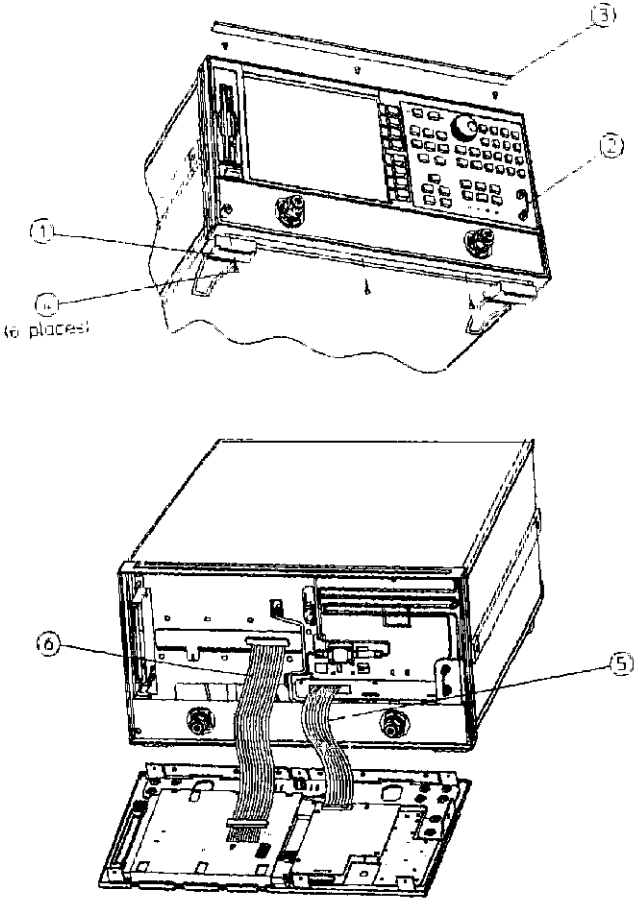
Removal

1. Disconnect the power cord.
2. Remove the front bottom feet (item 1).
3. Remove all of the RF cables that are attached to the front panel (item 2).
4. Remove the trim strips (item 3) from the top and bottom edges of the front frame by prying under the strip with a small slot screwdriver.
5. Remove the six screws (item 4) from the top and bottom edges of the frame.
6. Slide the front panel over the test port connectors.
7. Disconnect the ribbon cables (item 5) and (item 6). The front panel is now free from the instrument.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semi-rigid cables, it is recommended that the connections be torqued to 10 in-lb.



sb651d

Front Panel Interface and Keypad Assemblies

Tools Required

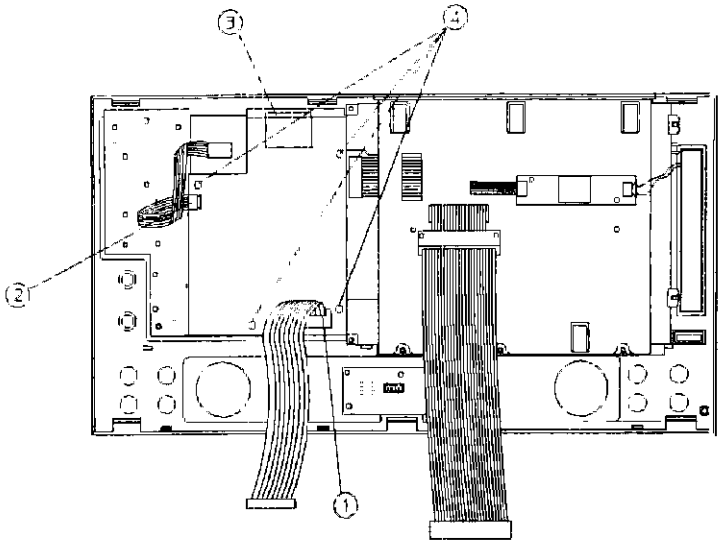
- T- 10 TORX screwdriver
- T- 15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

1. Remove the front panel assembly from the analyzer (refer to "Front Panel Assembly" in this chapter).
2. Remove the ribbon cable (item 1) from the front panel interface.
3. Disconnect the RPG cable (item 2) from the front panel interface.
4. Disconnect the ribbon cable (item 3) by sliding your finger nail between the connector and the cable.
5. Remove the four screws (item 4), attaching the interface board.
6. Remove the nine screws from the A1 front panel board to access and remove the keypad.

Replacement

1. Reverse the order of the removal procedure.



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Display Lamp and Assembly

Tools Required

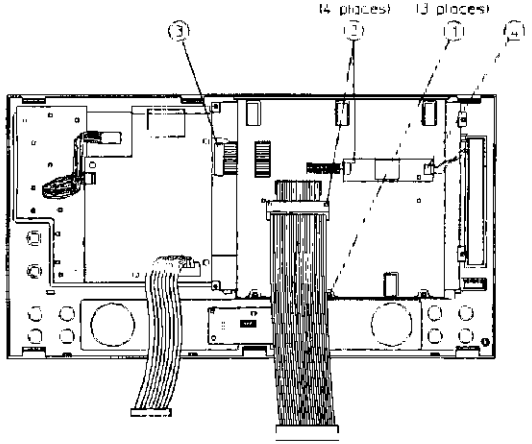
- T-10 TORX screwdriver
- T- 15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

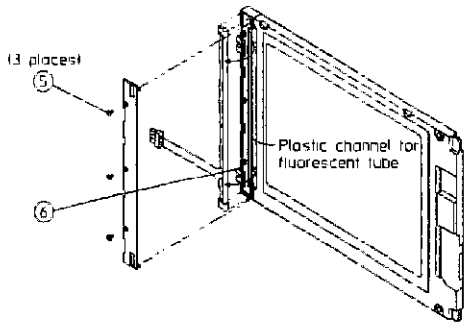
Removal

1. Remove the front panel assembly (refer to "Front Panel Assembly" in this chapter).
2. Remove the three screws (item 1) that attach the display to the front panel.
3. Remove the four screws (item 2), disconnecting the accessories from the display.
4. Disconnect the cable (item 3) from the A1 assembly.
5. Disconnect the display lamp cable (item 4).
6. Lift the display from the front panel and remove the three screws (item 5) from the outside of the display.
7. Pull the lamp (item 6) out with a curving side motion, as shown.

Replacement

1. Reverse the order of the removal procedure.


(4 places)
(3 places)
3
2
1
4


(3 places)
5
6
Plastic channel for fluorescent tube

Rear Panel Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

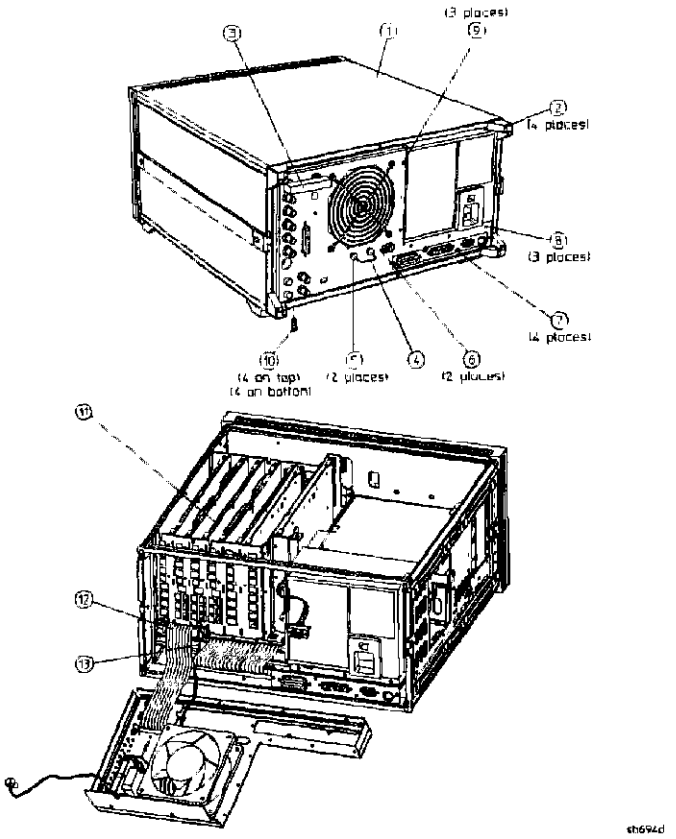
Removal

1. Disconnect the power cord and remove the top (item 1) and bottom covers (refer to "Covers" in this chapter).
2. Remove the four rear standoffs (item 2).
3. If the analyzer has option 1D5, remove the BNC jumper from the high stability frequency reference (item 3).
4. If the analyzer has option 085, remove the RF cable (item 4) and the connectors' attaching hardware (item 5).
5. Remove the hardware (item 6) that attaches the RS-232 connector to the rear panel.
6. Remove the four screws (item 7) that attach the interface bracket to the rear panel.
7. Remove the six screws (item 8) and (item 9), that attach the preregulator to the rear panel.
8. Remove the eight screws (item 10) from the rear frame: four from the top edge and four from the bottom edge.
9. Remove the screw from the pc board stabilizer and remove the stabilizer.
10. Lift the reference board (A12) from its motherboard connector and disconnect the flexible RF cable (item 11)

11. Pull the rear panel away from the frame. Disconnect the ribbon cable (item 12) from the motherboard connector, pressing down and out on the connector locks. Disconnect the wiring harness (item 13) from the motherboard.

Replacement

1. Reverse the order of the removal procedure.



Rear Panel Interface Board Assembly

Tools Required

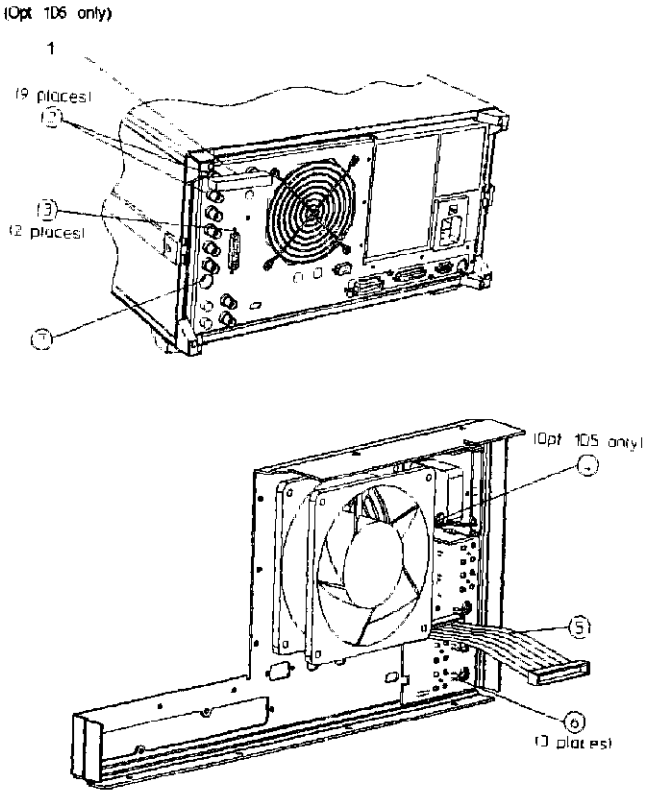
- T- 10 TORX screwdriver
- T- 15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top and bottom covers (refer to "Covers" in this chapter).
2. If the analyzer has option 1D5, remove the high-stability frequency reference jumper (item 1).
3. Remove the hardware that attaches the nine BNC connectors to the rear panel (item 2).
4. Remove the hardware that attaches the interface connector to the rear panel (item 3).
5. Remove the rear panel from the analyzer (refer to "Rear Panel Assembly" in this chapter)
6. If the analyzer has option 1D5, disconnect the cable (item 4) from the rear panel interface board.
7. Disconnect the ribbon cable (item 5) from the rear panel interface board.
8. Disconnect the wiring for the three BNC connectors and remove the attaching hardware (item 6).
9. Remove the MEAS RESTART connector from the interface board, approaching it from the outside of the rear panel assembly (item 7).

Replacement

1. Reverse the order of the removal procedure.



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Source Assemblies

Tools Required

- T- 15 TORX screwdriver
- 5/16-inch open-end torque wrench (set to 10 in-lb)
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the top cover (refer to "Covers" in this chapter).
2. Remove the front panel (refer to "Front Panel Assembly" in this chapter).
3. Remove the source module cover.

A58 M/A/D/S Removal

4. Disconnect the cables (item 2) and (item 3 for all but Option 400) from the M/A/D/S
5. Remove the four screws (item 6) from each corner of the assembly.

Oscillator Removal

6. Remove the three screws (item 1) that attach the source module to the analyzer.
7. Disconnect the cables (item 2) and (item 3 for all but Option 400) from the M/A/D/S.
8. Remove the four screws (item 4) and (item 5) from the source module bracket. Remove the bracket.
9. Lift the source module out of the analyzer.
10. Remove a screw (item 7) from the back of the oscillator.
11. Disconnect attaching RF cables.

A9 Source Control Board Removal

12. Remove the three screws (item 1) that attach the source module to the analyzer.
13. Disconnect the cables (item 2) and (item 3 for all but Option 400) from the M/A/D/S.
14. Remove the four screws (item 4) and (item 5) from the source module bracket. Remove the bracket.
15. Lift the source module out of the analyzer.
16. Remove three screws to detach the bottom source module cover.
17. Remove four screws that attach the source control board to the source module frame.
18. Place one hand on the top of the A9 board, with your thumb near the A58 M/A/D/S, to push the board. Place your other hand on the bottom side of the A9, with your thumb and index finger put through the drilled holes, to pull the board.

Replacement

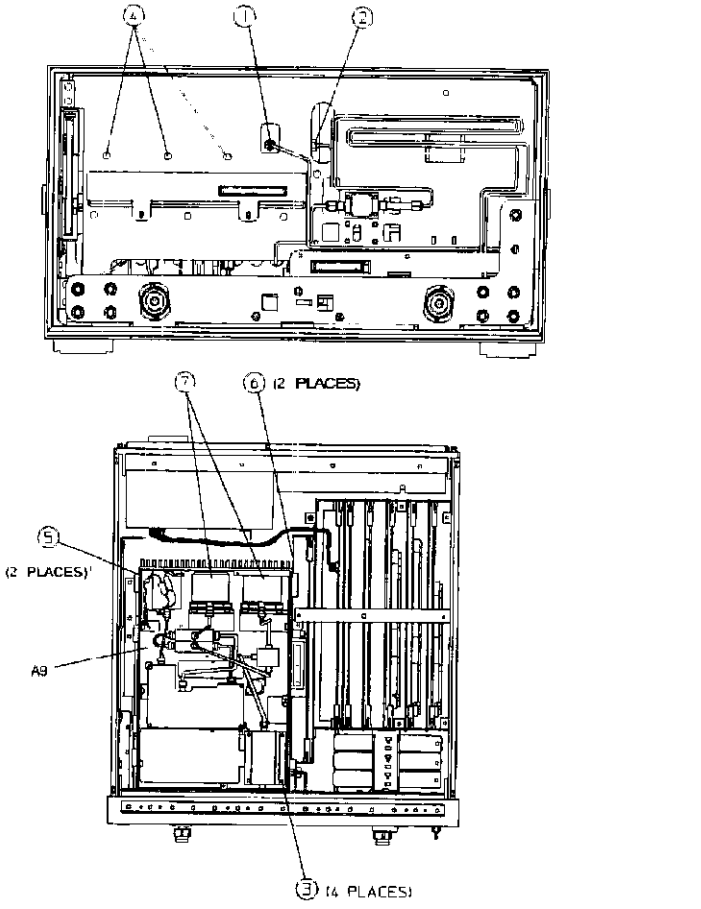
1. Reverse the order of the removal procedure.

Note

When replacing the A9 source control board, push the board evenly on all the microcircuit pins.

Check all the pin sockets from the back of the A9 board to ensure that all of the pins are inserted. For HP 8722Ds, you may need an eye glass to inspect the shallow pins of the SI high band switch.

When replacing the source module into the analyzer, push the cables aside before seating the module.



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A7 CPU Board Assembly

Tools Required

- T- 10 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1 Disconnect the power cord.

2. Remove the four bottom feet and bottom cover (refer to "Covers" in this chapter).

3. Remove the four screws (item 1) on the rear panel.

4. Turn the analyzer over and remove the screw (item 2) that secures the CPU board to the deck.

5. Disconnect the ribbon cable (item 3), sliding your finger nail between the cable and the connector.

6 Disconnect the ribbon cable (item 4) from the CPU board.

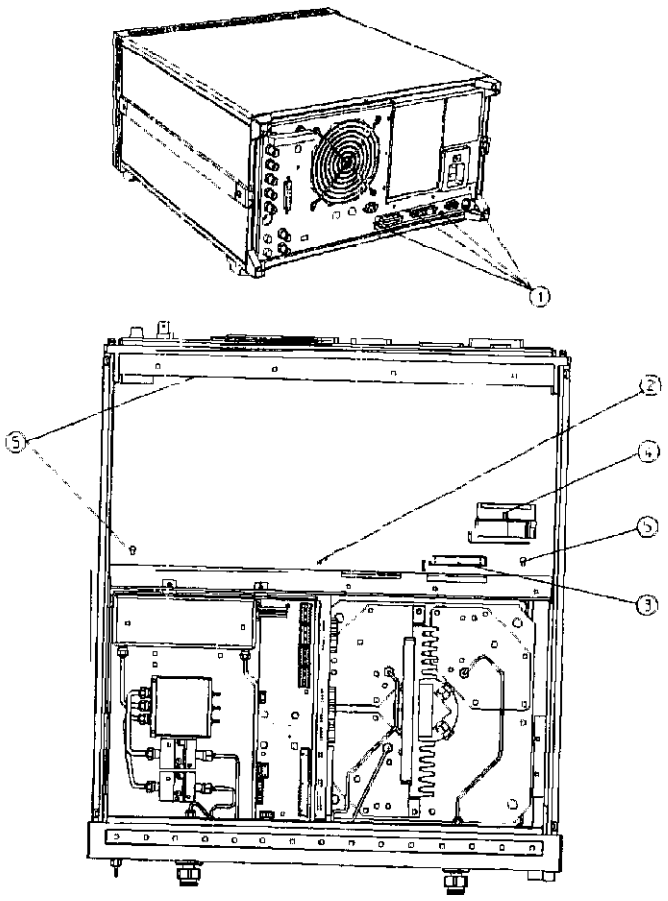
7 Slide the board towards the front of the instrument so that it disconnects from the three standoffs (item 5).

8. Disconnect the ribbon attached at the rear of the CPU board.

9. Lift the board off of the standoffs.

Replacement

1. Reverse the order of the removal procedure.



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A7BT1 Battery

Tools Required

- T- 10 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- soldering iron with associated soldering tools

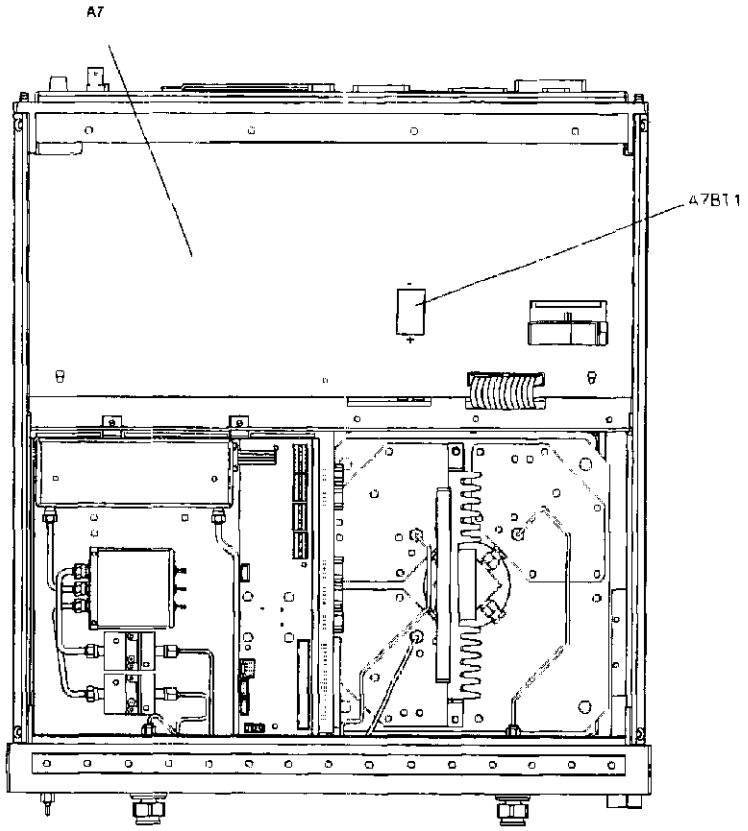
Removal

1. Remove the A7 CPU board (refer to "A7 CPU Board Assembly" in this chapter).
2. Unsolder and remove A7BT1 from the A7 CPU board.

Warning **Battery A7BT1 contains lithium. The battery may explode if it is incorrectly replaced. Do not incinerate or puncture this battery. Either dispose of the discharged battery, according to manufacturer's instructions, or collect as small chemical waste.**

Replacement

1. Make sure the new battery is inserted into the A7 board with the correct polarity.
2. Solder the battery into place
3. Replace the A7 CPU board (refer to "A7 CPU Board Assembly" in this chapter).



sb6118d

A15 Preregulator Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

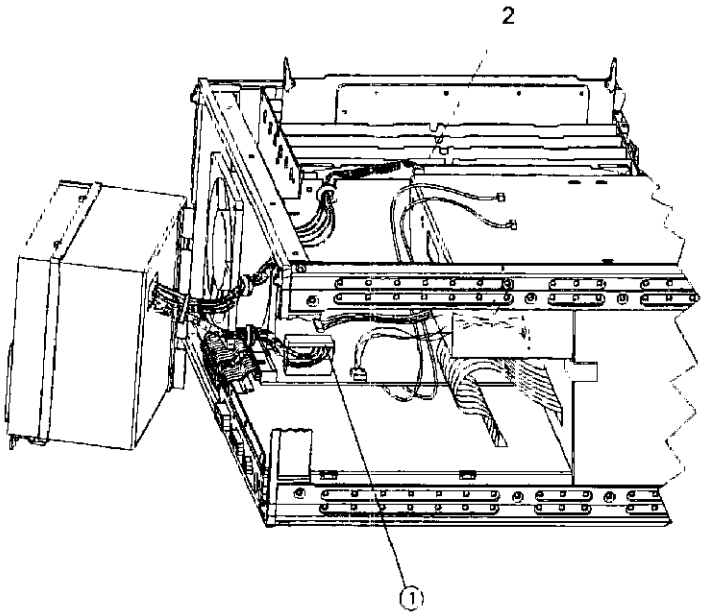
1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter)
2. Disconnect the wire bundles (item 1) (item 2) from the analyzer.
3. Remove the preregulator (A15) from the frame.

Replacement

1. Reverse the order of the removal procedure.

Note

- When reinstalling the preregulator (A15), make sure the three grommets on the wiring bundles are seated in the slots on the back side of the preregulator and also in the slot in the card cage wall.
- After reinstalling the preregulator (A15), be sure to set the line voltage selector to the appropriate setting, 115 V or 230 V.



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A19 Graphics Processor Assembly

Tools Required

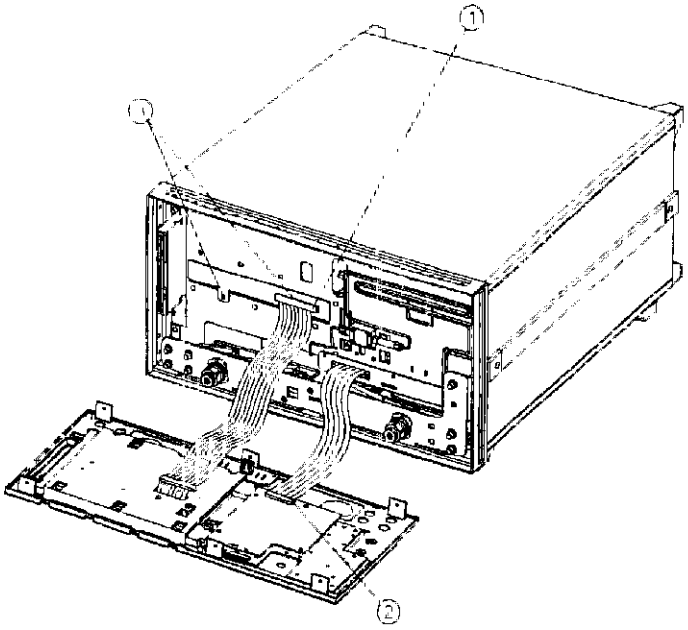
- T-10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the front panel (refer to "Front Panel Assembly" in this chapter).
2. Disconnect the two ribbon cables (item 1) and (item 2).
3. Remove the two screws (item 3) that attach the GSP to the front of the analyzer.
4. Pull the GSP board out of the analyzer.

Replacement

1. Reverse the order of the removal procedure.



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A3 Disk Drive Assembly

Tools Required

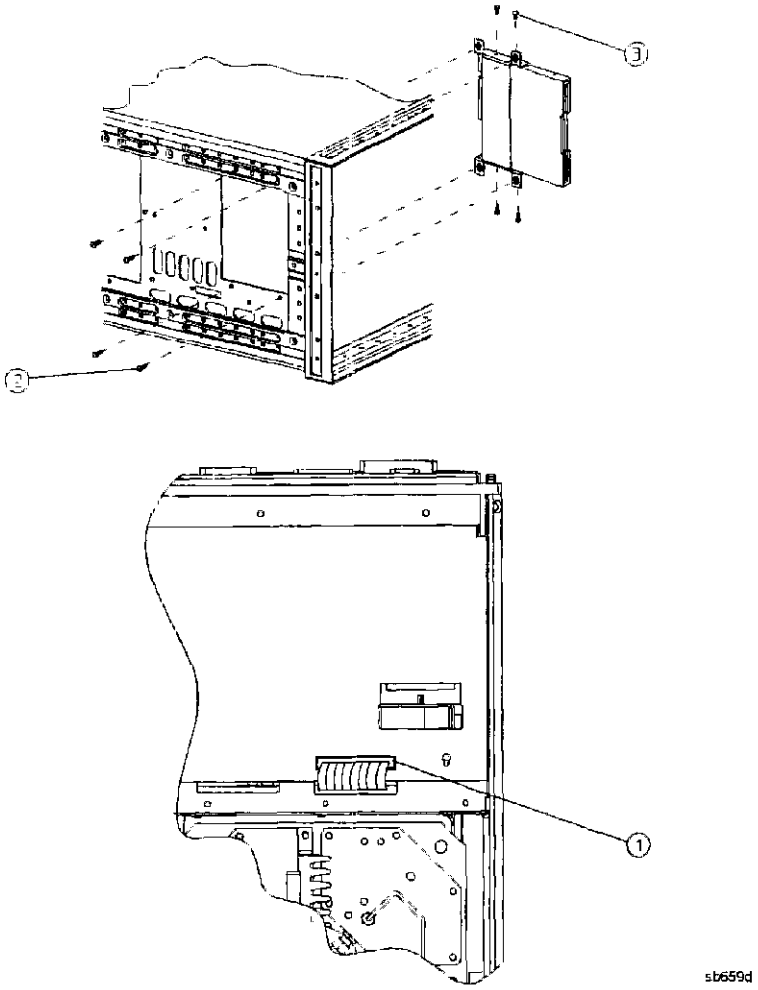
- T-8 TORX screwdriver
- T- 10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap

Removal

1. Disconnect the power cord and remove the bottom and left side covers (refer to "Covers" in this chapter).
2. Remove the front panel (refer to "Front Panel Assembly" in this chapter).
3. Turn the instrument upside-down and disconnect the ribbon cable, (item 1) from the CPU board.
4. Remove the four screws (item 2) that secure the disk drive bracket to the side of the frame.
5. Slide the disk drive out of the instrument.
6. Remove the four screws (item 3) that secure the disk drive to the bracket.

Replacement

1. Reverse the order of the removal procedure.


3
2
1
sb659d

A62, A63 Test Port Couplers and LED Board Assemblies

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- small slot screwdriver
- ESD (electrostatic discharge) grounding wrist strap
- 5/16-inch open-end torque wrench (set to 10 in-lb)

Removal

1. Remove the bottom cover (refer to "Covers" in this chapter).
2. Remove the front panel (refer to "Front Panel Assembly" in this chapter).
3. Reaching the connections from the bottom of the analyzer, disconnect the four RF cables attached to the couplers: two from the back of the couplers and two from between the couplers.
4. Remove the six screws (item 1) from the bottom edge of the front panel frame.
5. Remove one screw (item 2) from the right side of the coupler bracket.
6. Remove the coupler nuts (item 3).

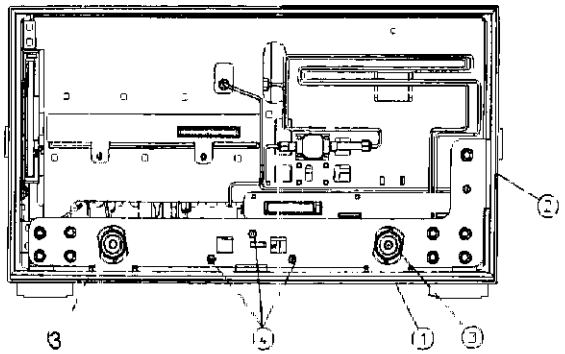
LED Board Removal

7. Remove the three screws (item 4) that attach the LED board to the coupler bracket.

Replacement

1. Reverse the order of the removal procedure.

Note When reconnecting semi-rigid cables, it is recommended that the connections be torqued to 72 in-lb.



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A26 High Stability Frequency Reference (Option 1D5) Assembly

Tools Required

- T-10 TORX screwdriver
- T-15 TORX screwdriver
- 9/16-inch hex-nut driver
- ESD (electrostatic discharge) grounding wrist strap

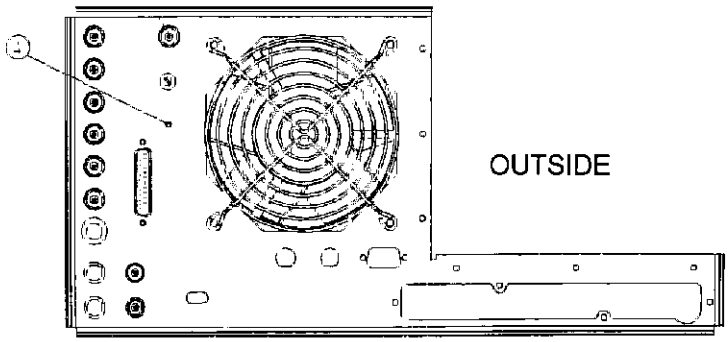
Removal

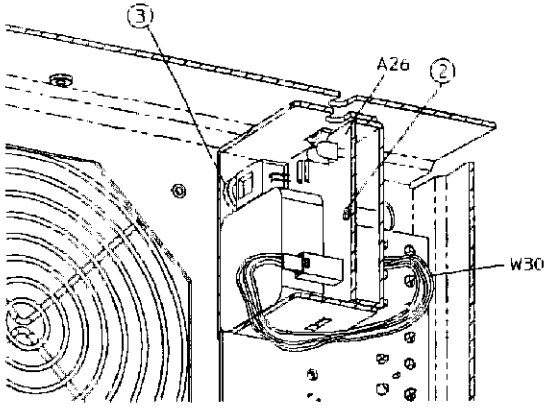
1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter).
2. Disconnect W30 from the high stability frequency reference board (A26).
3. Remove the BNC connector nut and washer from the "10 MHz PRECISION REFERENCE" connector (item 1) on the rear panel.
4. Remove the screw (item 4) that attaches the 1D5 assembly to the rear panel.
5. Remove the screw (item 2) that secures the high stability frequency reference board (A26) to the bracket.
6. Slide the board out of the bracket. Be careful not to lose the plastic spacer washer (item 3) that is on the BNC connector as the board is being removed.

Replacement

1. Reverse the order of the removal procedure.

Note Before reinserting the high stability frequency reference board (A26) into the bracket, be sure the plastic spacer washer (item 3) is on the BNC connector.





INSIDE

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B1 Fan Assembly

Tools Required

- 2.5-mm hex-key driver
- T- 10 TORX screwdriver
- T-15 TORX screwdriver
- ESD (electrostatic discharge) grounding wrist strap

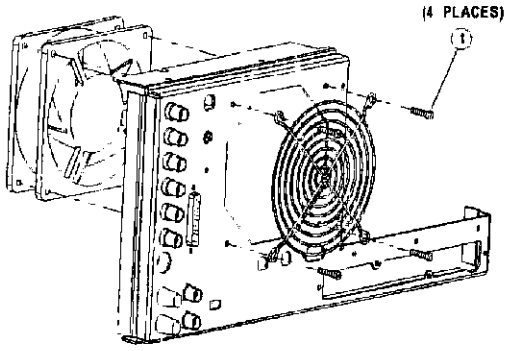
Removal

1. Remove the rear panel (refer to "Rear Panel Assembly" in this chapter).
2. Remove the four screws (item 1) that secure the fan and fan cover to the rear panel.

Replacement

1. Reverse the order of the removal procedure.

Note The fan should be installed so that the direction of the air flow is away from the instrument. There is an arrow on the fan chassis indicating the air flow direction.



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Post-Repair Procedures

The following tables list the additional service procedures which you must perform to ensure that the instrument is working correctly, following the replacement of an assembly. These procedures can be located in either Chapter 2 or Chapter 3.

Perform the procedures in the order that they are listed in the table.

Table 14-1. Related Service Procedures (1 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A1 Front Panel Keyboard	None	Internal Test 0 Internal Test 12 Internal Test 23 Internal Test 24
42 Front Panel Processor	None	Internal Test 0 Internal Test 12 Internal Test 23
A4/A5/A6 Second Converter	None	System Verification
452 Pulse Generator	Output Power Adjustments	System Verification
48 Post Regulator	None	Internal Test 0 Check A8 test point voltages
47 CPU[1]	A7 Jumper/Switch Positions Load Firmware[2] CC Retrieval Serial Number CC (Test 49) Option Number CC (Test 50) Display Intensity CC (Test 45) Analog Bus CC (Test 44) Source Pretune CC (Test 43) IF Amplifier CC (Test 47) EEPROM Backup Disk	Power Level Test Dynamic Range Test or System Verification

1 If you have an EEPROM backup disk available, you only need to perform the first five tests listed.

2 Only for instruments with firmware revisions 7 xx and above

Table 14-1. Related Service Procedures (2 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A9 Source Control	None	System Verification
A10 Digital IF	A7 Jumper/Switch Positions Analog Bus CC (Test 44) IF Amplifier CC (Test 47)	Dynamic Range Test System Verification Internal Test 17 Internal Test 18 Internal Test 19 or System Verification
A11 Phase Lock	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Source Pretune CC (Test 43)	Frequency Range and Accuracy or System Verification
A12 Reference	A7 Jumper/Switch Positions Reference Assembly VCO Tune Frequency Accuracy	Frequency Range and Accuracy
A13 Fractional-N (Analog)	A7 Jumper/Switch Positions Analog Bus CC (Test 44) Fractional-N Spur Avoidance and FM Sideband Adjustment	Internal Test 20 Frequency Range and Accuracy
A14 Fractional-N (Digital)	A7 Jumper/Switch Positions Analog Bus CC (Test 44)	Frequency Range and Accuracy Internal Test 20 or System Verification
A15 Preregulator	None	Self-Test†
A16 Rear Panel Interface	None	Internal Test 13, Rear Panel
A17 Motherboard	None	Self-Test†

† These tests are located in Chapter 4, "Start Troubleshooting Here"

Table 14-1. Related Service Procedures (3 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A18 Display	None	None
A19 Graphics System Processor	None	Observation of Display Tests 59-76*
A51 Test Set Interface	None	Operation Check†
A53 Low Band Assembly	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A54 YIG2 20-40 GHz (HP 8722D Only)	Source Pretune	Power Level Test Frequency Range and Accuracy
A55 YIG1 2 4-20 GHz	Source Pretune	Power Level Test Frequency Range and Accuracy
A56 Lower Front Panel Assembly	None	Observation (watch LEDs when switching from S11 to S22)
A57 Fixed Oscillator	Output Power Adjustments	Power Level Test Frequency Range and Accuracy
A58 M/A/D/S	Output Power Adjustments	Power Level Test
A59 Source Interface	Output Power Adjustments	Power Level Test
A60/61 DC Bias Tees	None	System Verification

* These tests are located in Chapter 6, "Digital Control Troubleshooting."
† These checks are located in Chapter 4, "Start Troubleshooting Here."

Table 14-1. Related Service Procedures (4 of 4)

Replaced Assembly	Adjustments/ Correction Constants (Ch. 3)	Verification (Ch. 2)
A62/A63 Directional Couplers	None	System Verification
A64 R1 Sampler	Sampler Check† Power Adjustment	System Verification Power Level Test
A64 R2 Sampler (Option 400 Only)	Sampler Check† Power Adjustment	System Verification Power Level Test
A65 A Sampler	Sampler Check†	System Verification
A66 B Sampler	Sampler Check†	System Verification
A68 6 dB Attenuator	None	Operation Check†
A69 Step Attenuator	None	Operation Check†
S1 Switch (HP 8722D Only)	None	Operation Check†
S2/S3 Switches	None	Operation Check†
S4 Transfer Switch	None	Operation Check†

† These checks are located in Chapter 4, "Start Troubleshooting Here."

Determining System Measurement Uncertainties

In any measurement, certain measurement errors associated with the system add uncertainty to the measured results. This uncertainty defines how accurately a device under test (DUT) can be measured.

Network analysis measurement errors can be separated into two types: raw and residual. The raw error terms are the errors associated with the uncorrected system that are called systematic (repeatable), random (non-repeatable), and drift errors. The residual error terms are the errors that remain after a measurement calibration.

The error correction procedure, also called measurement calibration, measures a set of calibration devices with known characteristics. It uses the measurement results to effectively remove systematic errors, using the vector math capabilities of the analyzer. The residual systematic errors remain after error correction, primarily due to the limitations of how accurately the electrical characteristics of the calibration devices can be defined and determined. Also, the random (non-repeatable) and drift errors, cannot be corrected because they cannot be quantified and measured during the measurement calibration and device measurement. However, the effects of random errors can be reduced through averaging. Random errors, that occur during a measurement calibration, are part of the error correction and become systematic errors when the calibration is turned on. For this reason, it is best to use a large number of averages during measurement calibration to reduce to the effect of the random errors. The averaging may then be reduced for device measurement. The residual systematic errors along with the random and drift errors continue to affect measurements after erro.correction, adding an uncertainty to the measurement results, Therefore, measurement uncertainty is defined as the combination of the residual systematic (repeatable), random (non-repeatable), and drift errors in the measurement system after error correction.

The following measurement uncertainty equations and system error models (flowgraphs) show the relationship of the systematic, random, and drift errors. These are useful for predicting overall measurement performance.

Sources of Measurement Errors

Sources of Systematic Errors

The residual (after measurement calibration) systematic errors result from imperfections in the calibration standards, the connector interface, the interconnecting cables, and the instrumentation. All measurements are affected by dynamic accuracy and frequency error effects. For reflection measurements, the associated residual errors are effective directivity, effective source match, and effective reflection tracking. For transmission measurements, the additional residual errors are effective crosstalk, effective load match, and effective transmission tracking.

The listing below shows the abbreviations used for residual systematic errors that are in the error models and uncertainty equations.

- Efd, Erd = effective directivity
- Efs, Ers = effective source match
- Efr, Err = effective reflection tracking
- Etc, Erc = effective crosstalk
- Efl, Erl = effective load match
- Eft, Ert = effective transmission tracking
- Crm, Ctm = cable stability (deg./GHz)
- Ab1, Ab2 = dynamic accuracy
- F = frequency

The sources for dynamic accuracy error effects are from errors during internal self-calibration routines, gain compression in the microwave frequency converter (sampler) at high signal levels, errors generated in the synchronous detectors, localized non-linearities in the IF filter system, and from LO leakage into the IF signal paths.

Sources of Random Errors

The random error sources are noise, connector repeatability and dynamic accuracy. There are two types of noise in any measurement system: low level noise (noise floor) and high level noise (phase noise of the source).

Low level noise is the broadband noise floor of the receiver which can be reduced through averaging or by changing the IF bandwidth.

High level noise or jitter of the trace data is due to the noise floor and the phase noise of the LO source inside the test set.

Connector repeatability is the random variation encountered when connecting a pair of RF connectors. Variations in both reflection and transmission can be observed.

The listing below shows the abbreviations used for random errors in the error models and uncertainty equations.

- Rnt = raw noise on trace (rms)
- Rnf = raw noise on floor (rms)
- Crrl = port 1 connector reflection repeatability error
- Crtl = port 1 connector transmission repeatability error
- Crr2 = port 2 connector reflection repeatability error
- Crt2 = port 2 connector transmission repeatability error

Sources of Drift Errors

Drift has two categories: frequency drift of the signal source and instrumentation drift. Instrumentation drift affects the magnitude and phase of both reflection and transmission measurements.

The primary causes for instrumentation drift are the thermal expansion characteristics of the interconnecting cables within the test set and the conversion stability of the microwave frequency converter.

The list below shows the drift errors in the error models and uncertainty equations.

- Dmxbx, Dmsax = drift magnitude
- Dpxbx, Dpsax = drift phase
- Dpfxbx, Dpfsax = drift phase/f

Sources of Additional Measurement Errors

Two additional categories of measurement errors are connection techniques and contact surfaces.

The connection techniques category includes torque limits, flush setting of sliding load center conductors, and handling procedures for beadless airlines.

The contact surfaces category includes cleaning procedures, scratches, worn plating, and rough seating.

These types of errors are not accounted for in the uncertainty analysis

Measurement Uncertainty Equations

Any measurement result is the vector sum of the actual test device response plus all error terms. The precise effect of each error term depends on its magnitude and phase relationship to the actual test device response. When the phase of an error response is not known, phase is assumed to be worst case (-180° to + 180°) Random errors such as noise and connector repeatability are generally combined in a root-sum-of-the-squares (RSS) manner.

Due to the complexity of the calculations, the performance verification/specifications software calculates the system measurement uncertainty. The following equations are representative of the equations the performance verification/specifications software uses to generate the system measurement uncertainty plots and tables.

Reflection Uncertainty Equations

Total Reflection Magnitude Uncertainty (Erm)

An analysis of the error model in Figure A-1 yields an equation for the reflection magnitude uncertainty, The equation contains all of the first order terms and the significant second order terms. The terms under the radical are random in character and are combined on an RSS basis. The terms in the systematic error group are combined on a worst case basis. In all cases, the error terms and the S-parameters are treated as linear absolute magnitudes.

$$\textit{Reflection magnitude uncertainty (forward direction)} =$$

$$Erm = Systematic + \sqrt{(Random)^2 + (Drift\ and\ Stability)^2}$$

$$Systematic = Efd + Efr\ S11 + Efs\ S11^2 + S21\ S12\ Efl + Ab1\ S11$$

$$Random = \sqrt{(Cr)^2 + (Rr)^2 + (Nr)^2}$$

$$Cr = \sqrt{(Crm1)^2 + (2Ctm1S11)^2 + (Crm1S11)^2 + (Crm2S21S12)^2}$$

$$Rr = \sqrt{(Crr1 + 2Crt1S11 + Crr1S11^2)^2 + (Crr2S21S12)^2}$$

$$Nr = \sqrt{(EfntS11)^2 + Efnf^2}$$

$$Drift\ and\ Stability = Dm1b1\ S11$$

where

- Efnt = effective noise on trace
- Efnf = effective noise floor
- Crtl = connector repeatability (transmission)
- Crrl = connector repeatability (reflection)
- Ctml = cable 1 transmission magnitude stability
- Crml = cable 1 reflection magnitude stability
- Crm2 = cable 2 reflection magnitude stability
- Dmsl = drift magnitude/±C source to port 1
- Efs = effective source match error
- Efr = effective reflection tracking error
- Efl = effective load match error
- Efd = effective directivity error
- Crr2 = Connector repeatability (reflection)

The detailed equation for each of the previous terms is derived from the signal flow model, located at the end of this appendix.

Reflection Phase Uncertainty (Erp)

Reflection phase uncertainty is determined from a comparison of the magnitude uncertainty with the test signal magnitude. The worst case phase angle is computed. This result is combined with the error terms related to thermal drift of the total system, port 1 cable stability, and phase dynamic accuracy.

$$Erp = Arcsin\left(\frac{Erm}{S11}\right) + 2Cpf1 \times f + Dps1 + Dpfs1 \times f$$

where

Cpf1 = cable phase/frequency port 1
Dps1 = drift phase/degree source to port 1
Dpfs1 = drift phase/degree/frequency source to port 1

Transmission Uncertainty Equations

Transmission Magnitude Uncertainty (Etm)

An analysis of the error model, located at the end of this appendix, yields an equation for the transmission magnitude uncertainty. The equation contains all of the first order terms and some of the significant second order terms. The terms under the radical are random in character and are combined on an RSS basis. The terms in the systematic error group are combined on a worst case basis. In all cases, the error terms are treated as linear absolute magnitudes.

$$\text{Transmission magnitude uncertainty (forward direction)} = Etm =$$

$$Ert = \text{Systematic} + \sqrt{(\text{Random})^2 + (\text{Drift and Stability})^2}$$

$$\text{Systematic} = Efc + (Ef_t + EfsS11 + EflS22 + EfsEflS21S12 + Ab2)\ S21$$

$$\text{Random} = \sqrt{(Ct)^2 + (Rt)^2 + (Nt)^2}$$

$$Ct = S21\sqrt{(Ctm1)^2 + (Ctm2)^2 + (Crm1S11)^2 + (Crm2S22)^2}$$

$$Rt = S21\sqrt{(Crt1)^2 + (Crt2)^2 + (Crr1S11)^2 + (Crr2S22)^2}$$

$$Nt = \sqrt{(EfntS21)^2 + Efnf^2}$$

$$\text{Drift and Stability} = Dm2b2S21$$

where

Crt2 = Connector repeatability (transmission) port 2
Crr2 = Connector repeatability (reflection) port 2
Efnt = effective noise on trace
Efnf = effective noise floor
Crr1 = connector repeatability (reflection)
Crt1 = connector repeatability (transmission)
Ctm1 = cable 1 transmission magnitude stability
Ctm2 = cable 2 reflection magnitude stability
Crm2 = cable 2 reflection magnitude stability
Dms1 = drift magnitude/°C source to port
Efs = effective source match error
Eft = effective transmission tracking error
Efl = effective load match error
Efc = effective crosstalk error

The detailed equation for each of the above terms is derived from the signal flow model, located at the end of this appendix.

Transmission Phase Uncertainty (Etp)

Transmission phase uncertainty is calculated from a comparison of the magnitude uncertainty with the test signal magnitude. The worst case phase angle is computed. This result is combined with the error terms related to phase dynamic accuracy, cable phase stability, and thermal drift of the total system.

$$Etp = Arcsin\ (\ Ert / S21\ ) + Cpf1 \times f + Cpf2 \times f + Dps1 + Dpfs1 \times f$$

where

Cpfl = Cable phase/frequency port 1
Cpf2 = Cable phase/frequency port 2
Dpsl = drift phase/degree source to port 1
Dpfsl = drift phase/degree/frequency source to port 1

Dynamic Accuracy

On the following page is a typical dynamic accuracy and noise curve for the analyzer. This curve is based on statistical samples of units built at the factory with an IF BW of 10 Hz.

Since this curve combines the effects of dynamic accuracy and noise, if used in uncertainty calculations, the effects of the noise terms in the corresponding equations can be eliminated

$$Dynamic\ Accuracy\ (linear) = 10^{\frac{\pm DynAcc(dB)}{20}} \pm 1$$

$$Dynamic\ Accuracy\ (dB) = 20log(\ 1 \pm Dynamic\ Accuracy\ (linear))$$

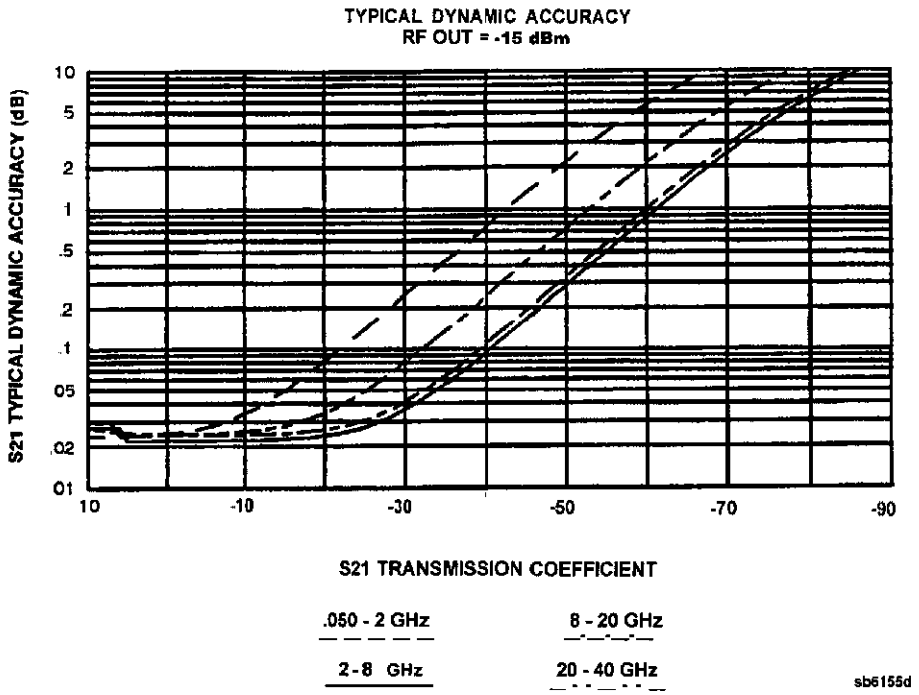

Figure A- 1. Typical Dynamic Accuracy

Determining Expected System Performance

Use the uncertainty equations, dynamic accuracy calculations in this appendix, and tables of system performance values from the "Specifications and Measurement Uncertainties" chapter in the *HP 8719D/20D/22D Network Analyzer User's Guide* to calculate the expected system performance. The following pages explain how to determine the residual errors of a particular system and combine them to obtain total error-corrected residual uncertainty values, using worksheets provided. The uncertainty graphs in the user's guide are examples of the results that can be calculated using this information.

Procedures

Use the measurement uncertainty worksheet to calculate the residual uncertainty in transmission and reflection measurements. Determine the linear values of the residual error terms and the nominal linear S-parameter data of the device under test as described below and enter these values in the worksheets. Then use the instructions and equations in the worksheets to combine the residual errors for total system uncertainty performance. The resulting total measurement uncertainty values have a confidence factor of 99.9%.

S-parameter Values. Convert the S-parameters of the test device to their absolute linear terms.

Noise Floor and Crosstalk. If a full 2-port calibration is performed, the residual crosstalk term can be ignored. Connect an impedance-matched load to each of the test ports and measure S21 or S12. Use the statistic function to measure the mean value of the trace. Use this value plus one standard deviation as the noise floor value of your system.

Dynamic Accuracy. Determine the absolute linear magnitude dynamic accuracy from the dynamic accuracy graph (see Figure A-1).

Other Error Terms. Depending on the connector type in your system, refer to residual error specifications in the "Specifications and Measurement Uncertainties" chapter in the *HP 8719D/20D/22D Network Analyzer User's Guide*, and the "Characteristic values Table" in this chapter to find the absolute linear magnitude of the remaining error terms.

Combining Error Terms. Combine the above terms using the reflection or transmission uncertainty equation in the worksheets.

Characteristic Values Table

	7 mm	3.5 mm	Type-N	2.4 mm
Crrl = Port 1 Reflection Connector Repeat	-65 dB	-60 dB	-60 dB	-60 dB
Crr2 = Port 2	-65 dB	-60 dB	-60 dB	-60 dB
Crt 1 = Port 1Transmission Connector Repeat	-65 dB	-60 dB	-60 dB	-60 dB
Crt2 = Port 2	-65 dB	-60 dB	-60 dB	-60 dB
Crm 1 -Cable Refl Mag Stability Port 1	-60 dB	-54 dB	-60 dB	-50 dB
Crm2-Cable Refl Mag Stability Port 2	-60 dB	-54 dB	-60 dB	-50 dB
Ctml -Cable Tran Mag Stability Port 1	±0.03 dB	±0 03 dB	±0 01 dB	±0 03 dB
Ctm2-Cable Tran Mag Stability Port 2	±0.03 dB	±0 03 dB	±0.01 dB	±0.03 dB
Cpf 1 -Cable Phase Stability Port 1 & Port 2	±0 09°/GHz	±0.09°/GHz	±0.1°/GHz	±0.09°/GHz
$D_{ms1,2}$-Magnitude Drift	0.0015°/°C	0 015°/°C	0.0015°/°C	0 0015°/°C
$D_{ps1,2}$ - Phase Drift	0.01°/°C	0 01°/°C	0.01°/°C	0 01°/°C
$D_{psf1,2}$ - Phase Drift with Temp & Frequency	0 15°/°C	0.15°/°C	0 15°/°C	0 15°/°C

Measurement Uncertainty Worksheet (1 of 3)

Error Term	Symbol	dB Value	Linear Value
S_{11}	S_{11}		
S_{21}	S_{21}		
S_{12}	S_{12}		
S_{22}	S_{22}		
Directivity	E_{fd}		
Reflection Tracking	E_{fr}		
Source Match	E_{fs}		
Load Match	E_{fl}		
Transmission Tracking	E_{ft}		
Effective Crosstalk	E_{fc}		
Dynamic Accuracy (Magnitude)	A_{b1}, A_{b2}		
Noise Floor	E_{fnf}		
High Level Noise	E_{fnt}		
Connector Reflection Repeatability Port 1	C_{rr1}		
Connector Transmission Repeatability Port 1	C_{rt1}		
Magnitude Drift Due to Temperature	$D_{ms1,2}$		
Phase Drift Due to Temperature	$D_{ps1,2}$		
Phase Drift Due to Temperature and Frequency	$D_{pfs1,2}$		
Cable Reflection Stability	C_{rm1}		
Cable Transmission Stability	C_{rm2}		
Connector Reflection Repeatability Port 2	C_{rr2}		
Connector Transmission Repeatability Port 2	C_{rt2}		
Cable Phase/Frequency Port 1	C_{pf1}		
Cable Phase/Frequency Port 2	C_{pf2}		

Magnitude
Combine Systematic Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors to obtain the total sum of systematic errors.

E_{fd}	_____=_____	(k)
$E_{fr} \times S_{11}$	_____x_____=_____	(l)
$E_{fs} \times S_{11} \times S_{11}$	_____x_____x_____=_____	(m)
$E_{fl} \times S_{21} \times S_{12}$	_____x_____x_____=_____	(n)
$A_{b1} \times S_{11}$	_____x_____=_____	(o)
Subtotal: k + l + m + n + o	_____+_____+_____+_____+_____=_____	(S)

Combine Random Errors. In the space provided, enter the approprii linear values from the list of errors. Then combine these errors in an RSS fashion to obtain a total sum of the random errors.

$(E_{fnt} \times S_{11})^2 + E_{fnf}^2$	(_____x_____)2 +_____=_____	(w^2)
$(C_{rr1}+2 \times C_{rt1} \times S_{11}+C_{rr1} \times S_{11}^2)^2$ $+(C_{rr2} \times S_{21} \times S_{12})^2$	(_____+2 x_____+_____x_____2)2 +(_____x_____x_____)2=_____	(x^2)
$C_{rm1}^2 + (2 \times C_{tm1} \times S_{11})^2$ $(C_{rm1} \times S_{11})^2 + (C_{rm1} \times S_{11})^2 +$ $(C_{rm2} \times S_{21} \times S_{12})^2$	_____2+(2 x_____x_____)2 + (_____x_____)2+(_____x_____)2 +(_____x_____x_____)=_____	(y^2)
$(D_{mb1} \times S_{11})^2$	(_____x_____)2=_____	(z^2)
$\sqrt{w^2+x^2+y^2+z^2}$	√ _____+_____+_____+_____ = _____	(R)
Subtotal: S + R	_____+_____=_____	(V_r)

Total Magnitude Errors:

E_{rm} (linear) = V_r	_____=_____	
E_{rm} (log) = Log (1±E_{rm}/S_{11})	20 Log (1± _____/_____)=_____	dB

Phase

E_{rp}=Arcsin (E_{rm}/S_{11})+2 x C_{pf1} x f +D_{ps1} + D_{pfs1} x f)	Arcsin(_____/_____)+2x_____+_____+_____=_____degrees	

Measurement Uncertainty Worksheet (3 of 3)

Magnitude

Combine Systematic Errors. In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors to obtain the total sum of systematic errors.

E_{fc}	_____ = _____	(k)
$E_{ft} \times S_{21}$	_____ x _____ = _____	(l)
$E_{fs} \times S_{11} \times S_{21}$	_____ x _____ x _____ = _____	(m)
$E_{fl} \times S_{22} \times S_{21}$	_____ x _____ x _____ = _____	(n)
$E_{fs} \times E_{fl} \times S_{21}^2 \times S_{12}$	_____ x _____ x _____ x _____ = _____	(o)
$A_{b2} \times S_{21}$	_____ x _____ = _____	(p)
Subtotal: k+l+m+n+o	_____ + _____ + _____ + _____ + _____ = _____	(S)

Combine Random Errors In the space provided, enter the appropriate linear values from the list of errors. Then combine these errors in an RSS fashion to obtain a total sum of the random errors.

$(E_{fnt} \times S_{21})^2 + E_{fnf}^2$	(_____ x _____)^2 x _____^{2} = _____	(w^2)
$S_{21}^2(C_{rt1}^2 + C_{rt2}^2 + (C_{rr1} \times S_{11})^2 + (C_{rr2} \times S_{22})^2)$	_____^{2}(_____^{2} + _____^{2} + (_____ x _____)^2 + (_____ x _____)^2) = _____	(x^2)
$S_{21}^2(C_{tm1}^2 + C_{tm2}^2 + (C_{rm1} \times S_{11})^2 + (C_{rm2} \times S_{22})^2)$	_____^{2}(_____^{2} + _____^{2} + (_____ x _____)^2 + (_____ x _____)^2 = _____	(y^2)
$(D_{m2b2} \times S_{21})^2$	(_____ x _____)^2 = _____	(z^2)
$\sqrt{w^2 + x^2 + y^2 + z^2}$	$\sqrt{\text{_____ + _____ + _____ + _____}}$ = _____	(R)
Subtotal: S + R	_____ + _____ = _____	(V_r)

Total Magnitude Errors:

E_{rm} (linear) = V_r	_____ = _____	
E_{rm} (log) = Log (1±E_{rm}/S_{11})	20 Log (1± _____ / _____) = _____	dB

Phase

E_{tp} = Arcsin (E_{tm}/S_{21}) + C_{pf1} x f + C_{pf2} x f + D_{ps1} + D_{pfs1} x f	Arcsin (_____ / _____) + _____ + _____ + _____ = _____	degrees